

## The Ramped-step Voltage in Adiabatic Logic Circuits: Analysis of Parameters to Further Reduce Power Dissipation

<sup>1</sup>Nazrul Anuar Nayan, <sup>2</sup>Yasuhiro Takahashi and <sup>2</sup>Toshikazu Sekine

<sup>1</sup>Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia, Bangi, Selangor, Malaysia

<sup>2</sup>Faculty of Engineering, Gifu University, Gifu, Japan

**Abstract:** Ramped-step voltage supplies are widely used in adiabatic switching. However, the set of analytical parameters available for understanding these voltage supplies is still limited. Our objective is to identify the parameters that have an effect on lowering power dissipation. Our results show that power dissipation can be significantly reduced using adiabatic logic, by increasing the charging and discharging times and by reducing the peak current flow through the transistors. The phenomenon of energy recovery is also demonstrated. A maximum of 40% reduction in the total power dissipation is shown from this analysis.

**Keywords:** Adiabatic logic, discharging, energy recovery, low-power

### INTRODUCTION

In conventional CMOS circuits, power dissipation primarily occurs during device switching. A sudden flow of current through channel resistive elements results in half of the supplied energy being dissipated at each transition. Low-power circuit systems achieved by implementing the concept of adiabatic switching (Athas *et al.*, 1994) and energy recovery have been applied and various energy-recovery circuits with adiabatic circuitry for ultra-low power implementation have been presented. In the circuit-level adiabatic technique, charge transfer occurs without the generation of heat. During adiabatic switching, all the nodes are charged or discharged at a constant current to minimize power dissipation. This is accomplished with a ramped-step voltage or an AC power supply to initially charge the circuit during specific adiabatic phases and then discharging the circuit to recover the supplied charge.

However, a thorough theoretical analysis of the ramped-step voltage has not been discussed to date in the literature. Zimmermann *et al.* (1997) accounted for only the dynamic power digital CMOS which depended on the supply voltage  $V_{dd}$ , the clock frequency  $f_{clk}$ , the node switching activities  $\alpha_n$ , the node capacitance  $c_n$ , the node short-circuit current  $i_{scn}$  and the number of nodes  $n$ . Alioto and Palumbo (2001) demonstrated the evaluation of the energy consumption by including the time constant  $T_{Di}$  and resistance between node  $i$  into the formula. Fischer *et al.* (2005) showed that the energy dissipation during the evaluation and recovery phases depends on the clock frequency; the on-resistance of the

MOSFET, the capacitance and the  $V_{dd}$ . Schlaffer (1996) demonstrated that decreasing the steepness of the ramp and thus increasing  $T$ , leads to decreasing dissipated energy.

In this study, adiabatic logic, which uses ramped-step volt-age is analyzed and compared with CMOS which utilizes step voltage. The objective is to identify the parameters that have an effect on further lowering power dissipation.

### CMOS CIRCUITS VIS-À-VIS ADIABATIC LOGIC CIRCUIT

**CMOS circuits:** As shown in Fig. 1, both pMOS and nMOS transistors can be modeled by including an ideal switch in series with a resistor to represent the effective channel resistance of the switch and the interconnect resistance.

The pull-up and pull-down networks are connected to the node capacitance  $C_L$ , which is referred to as the load capacitance in this study. When the logic level in the system is "1," there is a sudden flow of current through R:

$$Q = C_L V_{dd} \quad (1)$$

is the charge supplied by the positive power supply rail for charging the  $C_L$  to the  $V_{dd}$ . Hence, the energy drawn from the power supply is:

$$QV_{dd} = C_L V_{dd}^2 \quad (2)$$

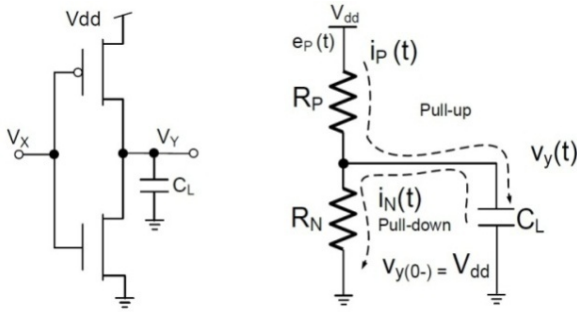


Fig. 1: A CMOS model showing an ideal switch in series with a resistor

If it is assumed that the energy drawn from the power supply is equal to that supplied to the  $C_L$ , the energy stored in the  $C_L$  becomes one-half the supplied energy, i.e.:

$$E_{\text{stored}} = \frac{1}{2} C_L V_{\text{dd}}^2 \quad (3)$$

The remaining energy is dissipated in  $R$ . The same amount of energy is dissipated during discharge in the nMOS pull-down network when the logic level in the system is “0”. Therefore, the total amount of energy dissipated as heat during charging and discharging is:

$$E_{\text{total}} = E_{\text{charge}} + E_{\text{discharge}} = \frac{1}{2} C_L V_{\text{dd}}^2 = C_L V_{\text{dd}}^2 \quad (4)$$

From the above equation, it is apparent that the energy consumption in a conventional CMOS circuit can be reduced by reducing the  $V_{\text{dd}}$ . By decreasing the switching activity in the circuit, the power consumption:

$$P = \frac{dE}{dt} \quad (5)$$

can also be proportionally suppressed.

**Adiabatic logic circuits:** Adiabatic switching is commonly used to minimize energy loss during charging/ discharging. The word “adiabatic” (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique.

Figure 2 shows the manner in which energy is dissipated during a switching transition in adiabatic logic circuits. In contrast to conventional charging, the peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfers over the

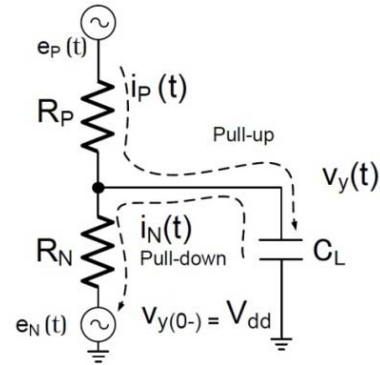


Fig. 2: Model of adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks

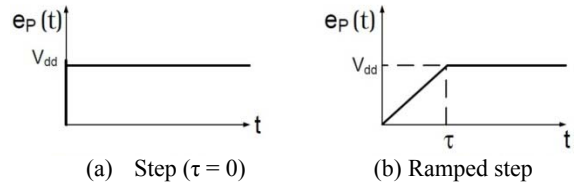


Fig. 3: Behavior of the pull-up network when the capacitor is charged to  $V_{\text{dd}}$ . (a) Step voltage and (b) ramped step voltage supply

entire length of time available because of the use of a time-varying voltage source instead of a fixed voltage supply. Hence, if  $I$  is the average current flowing to the  $C_L$ , the overall energy dissipation during the transition phase can be reduced in proportion as follows Seitz *et al.* (1985):

$$E_{\text{diss}} = \bar{I}^2 R \tau = \left( \frac{C_L V_{\text{dd}}}{\tau} \right)^2 R \tau = \left( \frac{R C_L}{\tau} \right) C_L V_{\text{dd}}^2 \quad (6)$$

Theoretically, during adiabatic charging, when the time  $T$  for the driving voltage  $e_P$  to change from 0 V to  $V_{\text{dd}}$  is long, the power dissipation is nearly zero. From Eq. (6), it is apparent that when power dissipation is minimized by reducing the current flow through the transistors, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it in subsequent computations. The signal energy may be recycled instead of dissipated as heat. It must be noted that systems based on the abovementioned theory of charge recovery are not necessarily reversible (Anuar *et al.*, 2010).

## PROPOSED MODEL

**Pull-up network:** Here, the power dissipation of two different voltage clocks is analyzed. The step voltage as it is used in the CMOS circuit and the ramped-step

voltage supply, which is used in the adiabatic switching circuit, as demonstrated in Fig. 3.

Let us consider the circuit diagram in Fig. 1. By these three equations of  $e_p(t)$ ,  $i_p(t)$  and initial condition of  $v_y(0_-)$ :

$$e_p(t) = R_P i_p(t) + v_y(t) \quad (7)$$

$$i_p(t) = C \left( \frac{d v_y(t)}{dt} \right) \quad (8)$$

$$v_y(0_-) = 0 \quad (9)$$

the instantaneous power dissipation at the power supply clock is derived as:

$$p_p(t) = \frac{V_{dd}^2}{R_P} e^{-\frac{t}{CR_P}} \quad (10)$$

Then, as the energy supplied at the power supply is:

$$w_p(t) = \int_0^t p_p(\tau) d\tau + w_p(0) \quad (11)$$

for the step voltage, by taking  $t$  to be infinity:

$$w_p(\infty) = CV_{dd}^2 \quad (12)$$

And for the ramped step voltage, by taking  $t$  to be infinity:

$$w_p(\infty) = \frac{CV_{dd}^2}{2} + \frac{R_P C^2 V_{dd}^2}{\tau} \left[ 1 - \frac{CR_P}{\tau} (1 - e^{-\frac{\tau}{CR_P}}) \right] \quad (13)$$

**Pull-down network:** Similar to the pull-up network, for the pull-down network, the common circuit equation for the equivalent circuit shown in Fig. 1 is derived below with the initial condition  $V_y(0_-) = V_{dd}$ . Figure 4 shows the voltage supply of the step and the ramped step during pull-down network analysis:

$$e_N(t) = R_N i_N(t) + v_y(t) \quad (14)$$

$$i_N(t) = C \frac{d v_y(t)}{dt} \quad (15)$$

$$v_y(0_-) = V_{dd} \quad (16)$$

The supplied energy at the voltage source for the step voltage is obtained by taking  $t = \infty$ :

$$w_p(\infty) = CV_{dd}^2 \quad (17)$$

The supplied energy at the voltage source for the ramped step voltage is:

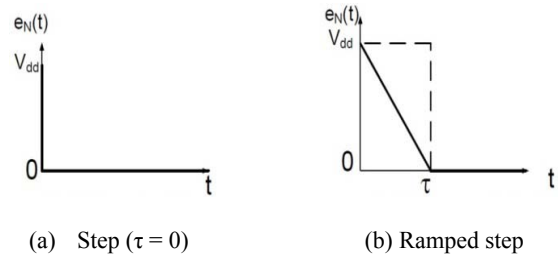


Fig. 4: The behavior of the pull-down network when the capacitor is charged to the  $V_{dd}$ . (a) Step voltage supply and (b) ramped-step voltage supply

$$w_p(\infty) = 2 \frac{R_N C^2 V_{dd}^2}{\tau} \left[ 1 - CR_N (1 - e^{-\frac{\tau}{CR_N}}) \right] \quad (18)$$

## RESULTS AND DISCUSSION

From the results of the analysis of Eq. (13) and (18), it is clearly shown that,  $\tau$  has a significant effect in reducing the energy dissipation, where the longer the  $\tau$ , the lower the dissipation in both the pull-up and pull-down networks using the adiabatic switching technique. From these analytical studies, comparison graphs have also been plotted in Fig. 5 to demonstrate the current flow into the transistor employing this scheme. Here, the pull up network is active from  $t = 0$  until  $t = 5$  s and the pull down network is used for  $t > 5$  s. As the area under the curve in Fig. 5 is related to the power dissipation or  $Ri^2$ , when the current is reduced, the total power dissipation is also decreased. From the graph, it is evident that the peak adiabatic circuit is lower and the total amount of current flow is smaller compared to CMOS. This theory has been implemented in Anuar *et al.* (2012) where power dissipation of 4x4-bit array multiplier using adiabatic switching, by simulation, is 55% lower than CMOS. This further supports the concept of low power dissipation in adiabatic switching circuits. The energy efficiency in adiabatic circuits is related to the on-resistance of both charge and discharge path.

In the energy dissipation graph of Fig. 6, the energy supplied,  $w_p$  in the CMOS step voltage, increases with time, but for the adiabatic ramped step voltage, there is a decrease after  $t = 5$  s when the energy,  $w_p$  in the circuit is delivered back to the power source. This is the phenomenon of energy recovery that occurs in adiabatic circuits. It is also obvious that the energy recovery can be increased by making the discharge time longer and/or the resistance at the nMOS is smaller. The dissipation at the resistive element,  $w_r$ , as shown by black solid color in the figure, can be reduced for the adiabatic case by increasing  $\tau$ . The dotted line

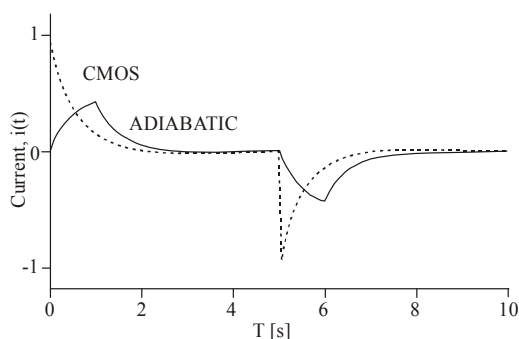


Fig. 5: Current flow comparison

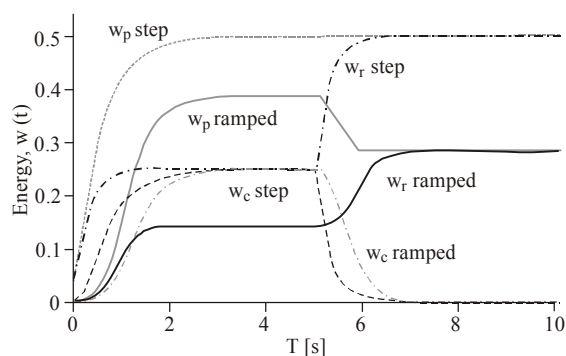


Fig. 6: Comparison of energy dissipation

representing the  $w_r$ , for the CMOS step voltage demonstrates that half of the total energy is dissipated during pull up and the other half is dissipated during pull down. From this graph, it is reconfirmed that the dissipation can be reduced by reducing the load capacitance and the voltage supplied. From Fig. 6, at  $t = 10s$ , the total energy of  $w_r$  and  $w_p$  for ramped-step voltage is 0.56 W, while for step voltage, this value is 1 W. Therefore, from this analytical study, up to 40% reduction of power dissipation per cycle is observed by implementing adiabatic switching circuit compared to conventional CMOS.

### CONCLUSION

In this study, it is clearly shown that the power dissipation in adiabatic logic circuits can be reduced by

increasing the charging and discharging times. It is also clearly shown that the lower the peak current flowing through the transistor, the lower the power dissipation. Energy recovery and reduction of peak currents during charging and discharging in adiabatic logic are clearly demonstrated. The concept of reducing the power dissipation by reducing both the load capacitance and/or the voltage supplied is also illustrated. Our analytical results show that energy recovery saves up to 40% of the total power dissipation in adiabatic logic circuits. The results in this study also reveal that power consumption in adiabatic logic circuits is considerably lower, which is advantageous for low-power digital applications.

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