Two Phase Clocked Adiabatic Static CMOS Logic

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***Abstract*—This paper demonstrates the low-energy operation of a two-phase clocked adiabatic static CMOS logic (2PASCL) on the basis of the results obtained in the simulation of a 4-bit ripple-carry adder (RCA) and D-flipflop employing 2PASCL circuit technology. Two-phase unsymmetrical power supply clocks are introduced to increase the logic transition level. Energy dissipation in the unsymmetrical clocked 2PASCL RCA and D-flipflop are 77.2% and 55.5% less than that in a static CMOS at transition frequencies of 10-100 MHz respectively.**

I. Introduction

Recently, clock and logic speeds have been increased for enhancing the performance of mobile and wireless devices; hence, it is important to design integrated circuits (ICs) that help achieve high energy efficiency. In recent years, adiabatic computing has been applied to low-power systems, and several adiabatic logic families have been proposed for low power logic applications [2]–[11]. The energy dissipated in adiabatic circuits is considerably less than that in static CMOS circuits; hence, adiabatic circuits are promising candidates for low-power circuits that can be operated in the frequency range in which signals are digitally processed. However, the diode-based adiabatic logic families [8]–[11] have several disadvantages such as low output amplitude and power dissipation across the diodes in the charging path.

A novel method for reducing energy dissipation in a quasi-adiabatic 2PASCL involves the design of a charging path without diodes. In this case, during charging, current flows only through the transistor. Thus, the 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through the diode and the transistor. With the aforementioned 2PASCL circuit, we can achieve high amplitude and reduce energy dissipation. In addition, to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

In this study, we introduce two unsymmetrical sinusoidal power supply clocks to increase the logic transition level in 2PASCL. We compare its power consumption to the previously proposed complementary clocks [12] and a conventional CMOS circuit. We simulate a simple logic circuit, an inverter, a 4-bit ripple-carry adder (RCA) [13] and D-flipflop using 2PASCL and CMOS circuit technologies.

II. CMOS Circuits vs. Adiabatic Logic Circuits

A. CMOS Circuits

Power dissipation in conventional CMOS circuits primarily occurs during the device switching. When the logic level in the system is "1," there is a sudden flow of current through R. $Q = C_L V_{dd}$ is the charge supplied by the positive power supply rail for charging C_L to the level of V_{dd}. Hence, the energy drawn from the power supply is $Q \cdot V_{dd} = C_L V_{dd}^2$ [4]. By assuming that the energy drawn from the power supply is equal to that supplied to C_L, the energy stored in C_L is said to be one-half the supplied energy, i.e., $E_{stored} = (\frac{1}{2}) C_L V_{dd}^2$. The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is $E_{charge} + E_{discharge} = C_L V_{dd}^2$.

From the aforementioned equation, it is apparent that energy consumption in a conventional CMOS circuit can be reduced by reducing V_{dd} and/or C_L. By decreasing the switching activity in the circuit, the power consumption ($P = \frac{dE}{dt}$) can also be proportionally suppressed.

B. Adiabatic Logic Circuits

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time-varying voltage source instead of a fixed voltage supply. This is accomplished by using AC power supplies to charge the circuit during the specific adiabatic phases and subsequently discharge the circuit to recover the supplied charge. The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfer over the entire time available. Hence, if $\hat{I}$ is considered as the average of the current flowing to C_L, the overall energy dissipated during the transition phase can be reduced in proportion to

$$\hat{I}^2 R T_p = \left(\frac{C_L V_{dd}}{T_p} \right)^2 R T_p = \left(\frac{R C_L}{T_p} \right) C_L V_{dd}^2. \quad (1)$$

Theoretically, during adiabatic charging, when T_p, the time for the driving voltage ϕ to change from 0 V to V_{dd} is long, energy dissipation is nearly zero.

When $\overline{\phi}$ changes from HIGH to LOW in the pull-down network, discharging via the nMOS transistor occurs. From Eq. (1), it is apparent that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors

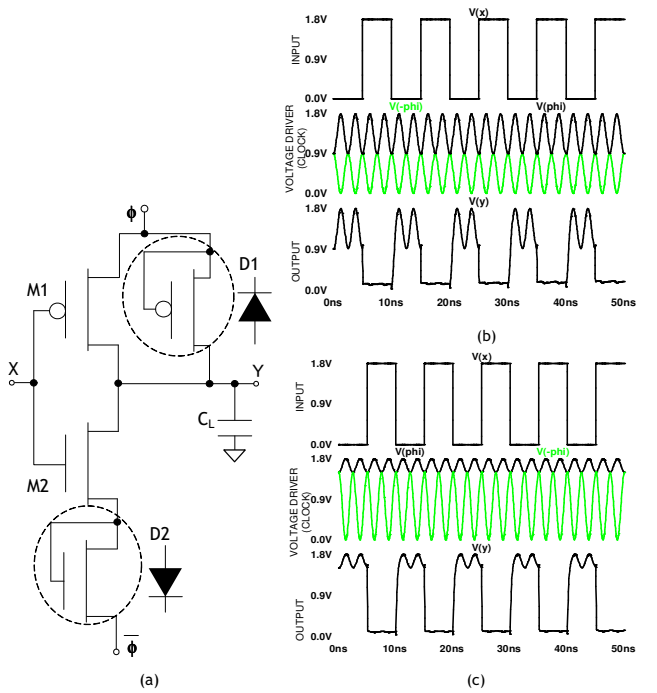

Fig. 1. (a) 2PASCL inverter circuit using (b) symmetrical power clocks, and (c) unsymmetrical power clocks from the simulation. Transition frequency X=100 MHz, ϕ = $\overline{\phi}$ = 400 MHz.

during a given computation step and uses it during subsequent computations. Systems based on the above-mentioned theory of charge recovery are not necessarily reversible.

III. 2PASCL

Figure 1 (a) shows a circuit diagram of 2PASCL inverter. A two-diode circuit is used, where one diode is placed between the output node and the power clock, and another diode is adjacent to the nMOS logic circuit and connected to another power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches. Figure 1 (b) and (c) show waveforms illustrating the operation of the 2PASCL inverter using symmetrical and unsymmetrical power clocks respectively.

The system uses a two-phase clocking split-level sinusoidal power supply, wherein ϕ and $\overline{\phi}$ replace V_{dd} and V_{ss}, respectively. One clock is in phase and the another is inverted. By using these two split-level sinusoidal waveforms, the voltage difference between the current-carrying electrodes can be minimized, and consequently power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to ϕ and GND respectively. From the previous design of complementary sinusoidal voltage driver clocks of each V_{p-p} being 0.9 V [12], we observed several fluctuations of the output waveforms especially at the HIGH state. This could affect the results when long cascading logic circuits are designed. To solve this problem, we introduce unsymmetrical split level sinusoidal power supply clocks as shown in 1 (c). For this unsymmetrical split level sinusoidal voltage drivers, the peak-to-peak voltage of ϕ and $\overline{\phi}$ are $V_{dd}/6$ and $5V_{dd}/6$. The voltage level of ϕ exceeds that of $\overline{\phi}$ by a factor of $V_{dd}/2.12$. The top graph shows the input signals, which are CMOS-compatible rectangular pulses. The middle graph shows the driving voltage of the split-level sinusoidal supply clock, and the last graph shows the output waveform.

The circuit operation is divided into two phases: *evaluation* and *hold*. In the *evaluation* phase, ϕ swings up and $\overline{\phi}$ swings down. On the other hand, in the *hold* phase, $\overline{\phi}$ swings up and ϕ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 1. The operation of the 2PASCL inverter is explained as follows.

1) *Evaluation* phase:
   a) When the output node Y is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor, and hence, the output is in the HIGH state.
   b) When node Y is LOW and nMOS is ON, no transition occurs.
   c) When the output node is HIGH and the pMOS is ON, no transition occurs.
   d) When node Y is HIGH and the nMOS is ON, discharging via nMOS and D2 causes the logic state of the output to be "0" [10].
2) *Hold* phase:
   a) When node Y is LOW and the nMOS is ON, no transition occurs.
   b) At the point when the preliminary state of the output node is HIGH and the pMOS is ON, discharging via D1 occurs.

The number of dynamic switching transition occuring during the operation of the 2PASCL circuit decreases as the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Because of this, node switching activities are suppressed to a significant extent and consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave as a static logic circuit.

IV. Simulation Results and Discussion

The simulation in this study was performed using SPICE circuit simulator with a 0.18-μm, 1.8-V CTX CMOS process. The width and length, W/L of nMOS and pMOS logic gates used were 0.6 μm/0.18 μm. A load capacitance (C_L) of 0.01 pF was connected to the output node Y. The frequency of the power supply clock was set to a value exactly four times the transition frequency. Simulations were carried out for the following purposes: the frequency characteristics of power consumption for the 2PASCL inverter in comparison to the other adiabatic logics including CMOS, and 2PASCL 4-bit RCA and D-flipflop circuits power consumptions in comparison with those obtained using CMOS circuits. The power consumption is calculated by integrating the product of voltage and current; $P = \frac{1}{T_s}\int_0^{T_s}\left(\sum_{i=1}^{n}(V_{pi} \times I_{pi})\right)dt$,

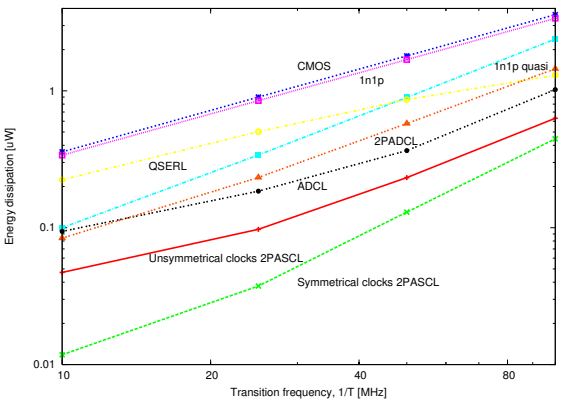

Fig. 2. Energy dissipation comparison of adiabatic inverters at different transition frequency.

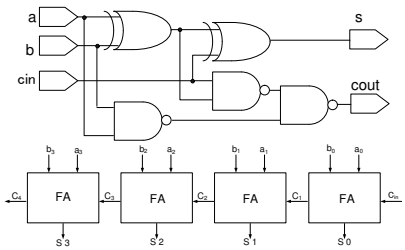

Fig. 3. Full Adder (FA) (top), and 4-bit Ripple Carry Adder (RCA) (bottom).

where T_s is the period of the primary input signal; V_p, is the power supply voltage; I_p, the power supply current; and n, the number of power supply [10].

A. Adiabatic inverters

For the first simulation, we compared the power dissipation in 2PASCL inverters with other adiabatic logics which are easily derived from CMOS. We also included CMOS inverter as a comparison. The adiabatic logics used in this comparison are 1n1p [6], 1n1p with split-level driving pulse [7], Quasi-Static Energy Recovery Logic (QSERL) [8], Adiabatic Dynamic CMOS Logic (ADCL) [9] and 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL) [10].

From the results shown in Fig. 2, the 2PASCL with symmetrical power clocks shows the lowest in energy dissipation followed by the 2PASCL with unsymmetrical power clocks.

B. 4-Bit RCA

To verify the practical applicability of the proposed 2PASCL circuit, we designed and simulated a 4-bit ripple carry adder. As shown in Fig. 3 (bottom), RCA consists of full adders (FA) which can be built by XOR and NAND gates as demonstrated on the top diagram of the same figure. In this study, we investigated logic functions and energy dissipation of a 4-bit RCA. RCA was chosen as it has a longer propagation path than do other adders.

The NAND, NOR and XOR logics based on 2PASCL are as shown in Fig. 4.

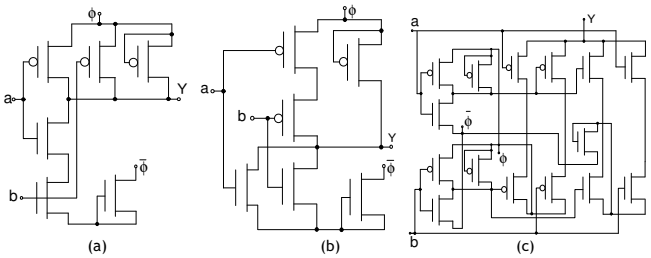

Fig. 4. Schematic for 2PASCL (a) NAND (b) NOR, and (c) XOR logics.

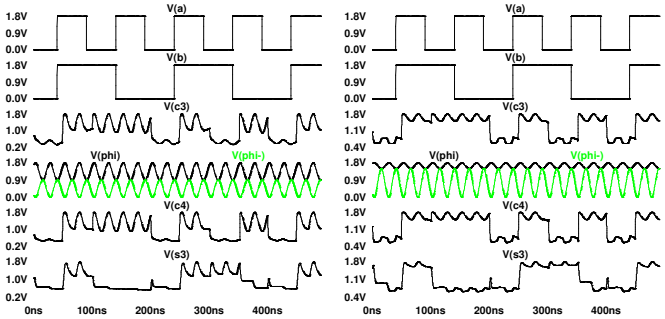

Fig. 5. Output waveforms for ripple carry adder of 2PASCL; using symmetrical power clocks (left), and unsymmetrical power clocks (right), from the simulation result of 10 MHz transition frequency. ($a_0 = a_1 = a_2 = a_3$, $b_0 = b_1 = b_2 = b_3$).

The SPICE simulation results obtained for the 4-bit 2PASCL RCA are shown in Fig. 5. We confirmed the functionality of the circuit. Compared to symmetrical power clocks, the fluctuations at the output HIGH state in unsymmetrical clocks have also been reduced. From the results, it is apparent that energy dissipation is much less in both 2PASCL RCA circuits with the split level sinusoidal clocking voltage than in the conventional static CMOS RCA when the simulated transition frequency is 10-100 MHz as shown in Fig. 6. Unsymmetrical clocks used in 4-bit RCA shows lower dissipation than the symmetrical power clocks.

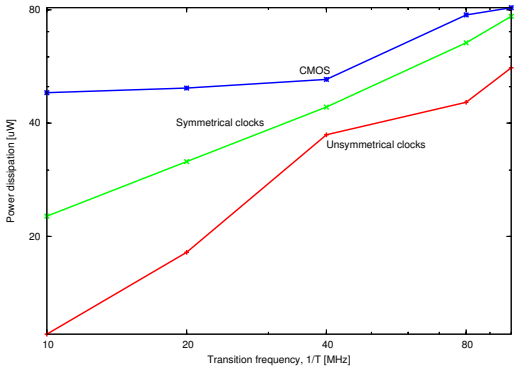

Fig. 6. Energy dissipation comparison of 2PASCL 4-bit RCA, and CMOS 4-bit RCA at different transition frequency.

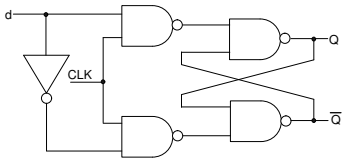

Fig. 7. D-flipflop.

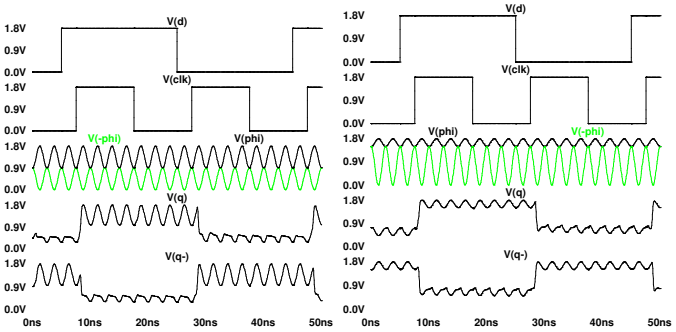

Fig. 8. Output waveforms comparison of 2PASCL D-flip flop with symmetrical complementary clocks (left), and unsymmetrical complementary clocks (right) at 100 MHz transition frequency.

C. D-flipflop

Next, we designed and simulated D-flipflop (DFF). As shown in Fig. 7, D-flipflop consists of NOT and NAND gates. Functionality of DFF and the waveforms from the simulations for symmetrical and unsymmetrical power clocks are illustrated in Fig. 8. The energy dissipation comparison is as demonstrated in Fig. 9.

V. Discussion

While the 2PASCL circuit has advantages such as low power dissipation and high fan out, its main disadvantage is floating outputs, which are attributed to the alternate hold phases that exist during the circuit operation [14]. Furthermore, there is a risk of current leakage (although small) as the gates are slowly switched ON. These problems will be addressed in our future research. The configuration of the two complementary low-power split-level sinusoidal power supply clocks is not discussed in this paper. The design of the power supply circuit will be proposed in a future study.

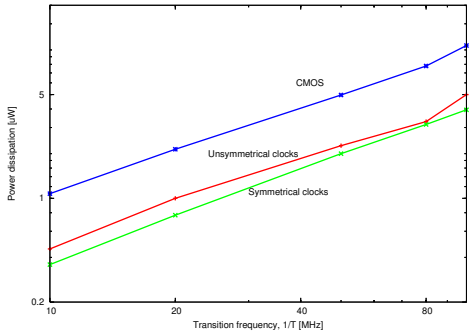

Fig. 9. Energy dissipation comparison of 2PASCL D-flipflop using symmetrical, unsymmetrical power clocks, and CMOS at different transition frequency.

VI. Conclusion

This paper describes the simulation of the 2PASCL inverters, 4-bit RCA and D-flipflop and their comparisons with CMOS on the basis of adiabatic charging and energy recovery. The simulation results show that power consumption in all 2PASCL inverters, RCA and D-flipflop are considerably less than that in a CMOS RCA. For the newly proposed unsymmetrical split level sinusoidal power clocks, the 2PASCL RCA dissipates only 22.8% of the energy dissipated by a static CMOS RCA at 10-100 MHz transition frequencies. For D-flipflop, the 2PASCL dissipates nearly half of the energy dissipated by a static CMOS. We also solve the fluctuation of the waveforms by implementing the unsymmetrical clocks; hence increasing the logic swings. Comparisons of the present results with those obtained for the simulation of 2PASCL circuit reveal that the proposed adiabatic logic circuits are advantageous for ultra low-energy computing applications.

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