A 4-bit Multiplier Using a Two Phase Drive Adiabatic Dynamic CMOS Logic

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Abstract: This paper describe the design and VLSI implementation of a multiplier using an adiabatic logic which is called a two phase drive adiabatic dynamic CMOS logic (2PADCL) circuit. Circuit operation and performance has been evaluated using a 4×4-bit 2PADCL multiplier fabricated in a 1.2 μm CMOS process. The experimental results show that the multiplier was operated with clock frequencies 800kHz. The total power dissipation of the 4×4-bit 2PADCL multiplier was also 5.19 mW at the 1.5 VDC power supply voltage.

1. Introduction

As operating frequencies and circuit densities have increased, energy dissipation and power flux has become problematic in a wide variety of digital devices, ranging from small portable system (e.g. personal digital assistant). The power consumption influences especially the battery life of the PDA. The adiabatic (or energy-recovering) logic is a new promising approach, which has been originally developed for low power digital circuits [1]–[6]. In [6], we proposed a new topology for the adiabatic circuit, which is called a two phase drive adiabatic dynamic CMOS logic (2PADCL). The 2PADCL has been achieved ultra low energy dissipation by restricting current to flow across devices with low voltage drop.

In this paper, we describe a VLSI implementation of a 4×4-bit multiplier using a 2PADCL circuit technology. The basis of the logic is presented in Section 2. In Section 3, we verify that carrying out design, trial manufacture and evaluation using the 2PADCL circuit actually, in respect of the 4×4-bit multiplier integrated circuit. The conclusions are summarized in Section 4.

2. Adiabatic Logic

2. 1. Adiabatic Charging

The main idea in an adiabatic charging is that transitions are considered to be slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver or oscillator. If a constant current source delivers the charge $Q=C_L V_{DD}$ during the time period ΔT, the energy dissipation in the channel resistance R is given by $E_{diss}=(C_L V_{DD}/\Delta T)^2\times(R\Delta T)$, where C_L is a load or internal capacitor, and V_{DD} is a DC power supply voltage. The above equation indicates that when the charging period ΔT is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic charging [1].

2. 2. 2PADCL

The 2PADCL inverter is shown in the top of Fig. 1, where the inverter is operated with complementary phases of power supply signals. The supply waveform consists of two modes, "evaluation" and "hold," as shown in the bottom of Fig. 1. Let us consider the adiabatic mode. When V_p and $\underline{V}_p$ are in evaluation mode, there is conducting path(s) in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged, which resembles to the CMOS circuit. Thus, there is no need to restore the node voltage to zero (or V_{DD}) every cycle. When V_p and $\underline{V}_p$ are in hold mode, Output node holds its value in spite of the fact that V_p and $\underline{V}_p$ are changing their values. We can find that such is the case by observing the function of diodes and the fact that the inputs of a gate have a different phase with the output. Circuits node are not necessarily charging and discharging every clock cycle, reducing the node switching activity.

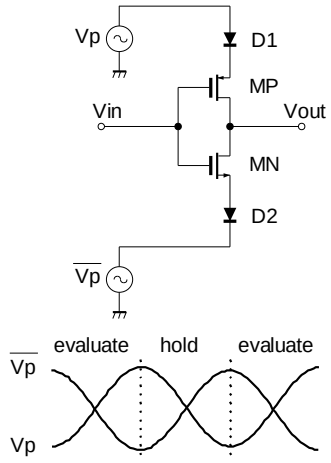

Figure 1. 2PADCL inverter. Structure and power supply.

3. 4×4-bit Multiplier Fabrication of 2PADCL

The simplest parallel multiplier is such that pairs of an AND gate and a 1-bit full adder are laid out repetitively and connected in sequence to construct an $n\times n$ array. Basic array multipliers consume low power and exhibit relatively good performance. In this study, we use a Braun's parallel array multiplier [7].

In order to validate the functionality of the 2PADCL logic and evaluate its performance, a 4×4-bit parallel carry-ripple array multiplier has been implemented in a 1.2 μm double-metal and double-poly CMOS n-well technology.

This chip size is 2.3×2.3 mm^2. The transistor size ratio W/L is 5.0 μm/1.2 μm for both of the PMOS and the NMOS transistors. The LSI has a total area of 926×704 μm^2, and its photomicrograph can be seen in Fig. 2.

Figure 3 displays the results of measurement using a digital oscilloscope. In the experiment, the supply voltage and clock frequency are as follows: 1) supply voltage V_{DD}: 5 VDC, 2) supply voltage V_p, $\underline{V}_p$: 5 V, 10 MHz, sine wave, 3) clock frequency f: 5 V, 800 kHz, square wave. In this figure, the total critical delay path includes the delay of input and output buffers. The experimental results show that the multiplier is operated with clock frequencies up to 800kHz.

In order to verify the power dissipation of a 4×4-bit multiplier, we used the power supply circuit illustrated in Fig. 4. This circuit is based on the Clapp oscillator that generates the sinusoidal voltage. This circuit is realized by using discrete components. The frequency of V_p is controlled to be near 10 MHz by adjusting the element values of L or C.

The oscillator circuit shown in Fig. 4 is connected to the 4×4-bit 2PADCL multiplier for supplying the power and thus, the 2PADCL system is constructed. The 2PADCL system is experimentally confirmed to operate perfectly. Dependency of the 2PADCL system power dissipation on the DC power supply voltage is shown in Fig. 5. From the figure, we can find that the 2PADCL system can operate with sub-one volt DC power supply. The power dissipation is also 5.19 mW at the 1.5 VDC power supply voltage.

4. Conclusions

In this paper, the 4×4-bit 2PADCL multiplier has been implemented by using a 1.2 μm CMOS process technology with the area of 926×704 μm^2. The experimental results have shown that the adiabatic multiplier is operated with clock frequencies up to 800 kHz, and the total power dissipation is also 5.19 mW including the power supply.

References

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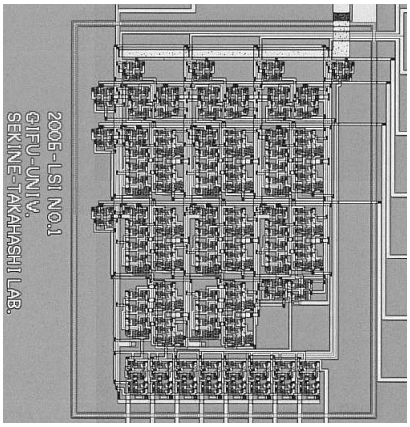

Figure 2. Photomicrograph of a 4×4-bit multiplier.

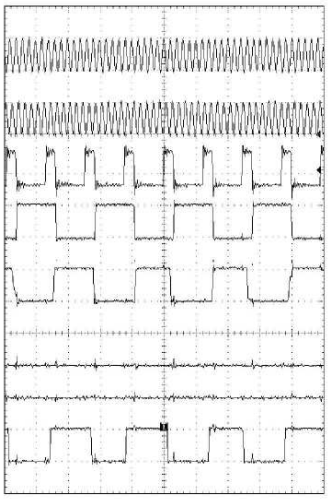

Figure 3. Measurement results of a 4×4-bit multiplier.

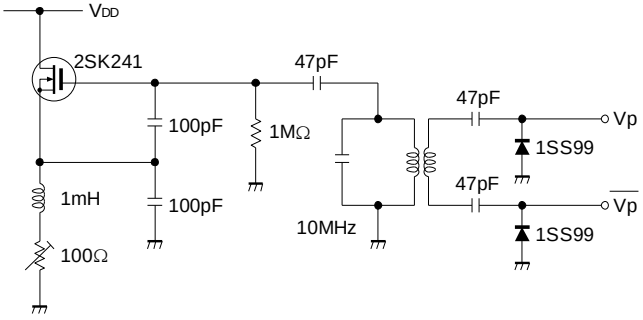

Figure 4. Clapp Oscillator for supplying the power.

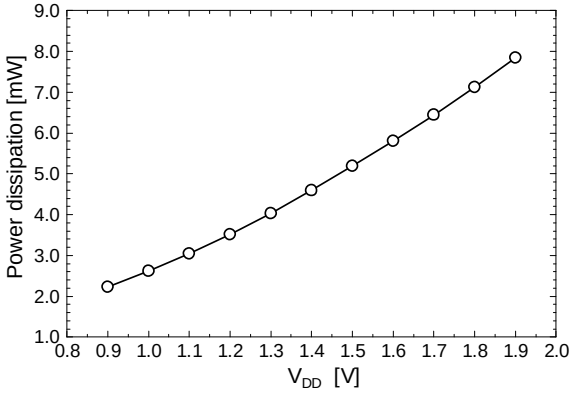

Figure 5. Dependency of the 2PADCL system power dissipation on the DC supply voltage.