A 70 MHz Multiplierless FIR Hilbert Transformer in 0.35 μm CMOS

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Abstract —— This paper presents the design and implementation of a 31-tap FIR Hilbert transform digital filter chip. The architecture is based on a computation sharing multiplier using vertical and horizontal common subexpression elimination techniques. A 31-tap FIR Hilbert transform digital filter was implemented and fabricated in CMOS 0.35 μm technology. The chip's core contains approximately 33k transistors and occupies 0.86 mm^2. The chip also has an operating speed of 70 MHz over.

1. Introduction

Because the digital Hilbert transformer is required to strictly shift the phase of signal by 90 degrees over wide range frequency, we generally have the choice of using FIR with linear phase [1]–[4].

The Hilbert transformer using FIR filter is attributable to its amplitude ripple and large circuit scale. The primary source of complexity in the FIR Hilbert transformer is the filter coefficients. If these coefficients have been represented in Canonic Signed Digit (CSD) format and implemented as constant multipliers, then we can save the circuit scale of Hilbert transformer [5].

In this paper, we present high performance implementations for digital Hilbert transformers based on our recently proposed constant multiplier [6], [7].

2. Hilbert Transform

The impulse response sequence of an ideal Hilbert transform is given as:

$$h(n) = \begin{cases} \dfrac{\sin^2(\pi n/2)}{\pi n/2} & \text{for} \quad |n| > 0 \\ 0 & \text{for} \quad n = 0. \end{cases} \qquad (1)$$

Note that $h(n) = 0$ for all even n and $h(-n)$, facts which are exploited in order to reduce the required circuitry. Of course, the ideal transform is not physically realizable since it is non-causal and infinite duration. In order to create a realizable filter, the impulse response is windowed and shifted to make it casual.

3. FIR Hilbert Transformer Chip Architecture

Multiple constant multiplication (MCM) can be implemented efficiently by using dedicated shift and add multipliers. Common subexpression elimination (CSE) as a way to tackle the MCM problems is as a possible method for the optimization

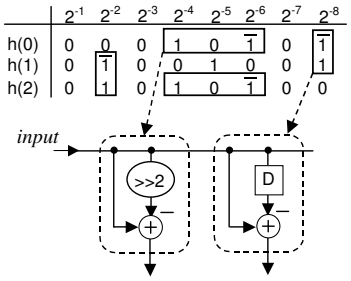


Figure 1. Proposed CSE in FIR filter design. $\overline{1}$ denotes -1. $>>$ is a bit shift operation.

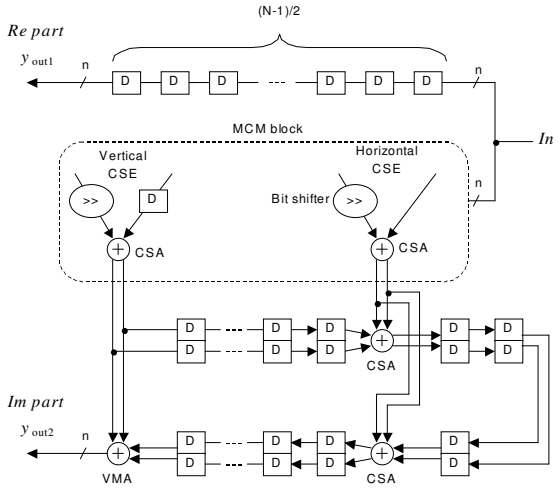


Figure 2. Final FIR Hilbert transformer structure.

of finite-duration FIR filter area through the reduction of the multiplier block logic. In general, the goal of CSE can be defined as follows: (1) Identify multiple patterns in the coefficient set. (2) Remove these patterns and calculate them only once. Our CSE techniques [6], [7] have been proposed an efficient way to find the correct bit-patterns for horizontal and vertical CSEs. The idea of the proposed CSE can be demonstrated on a FIR filter design shown in Fig. 1. The proposed CSE is stated as the problem of minimizing the numbers of the delay and adders/subtracter blocks which are needed to perform all of the multiplications. Using the proposed method, we can reduce the MCM area of the Hilbert transform filter by an average 20%. By using the MCM structure, we get the final FIR Hilbert transformer structure shown in Fig. 2, which requires a smaller chip size, a faster speed,

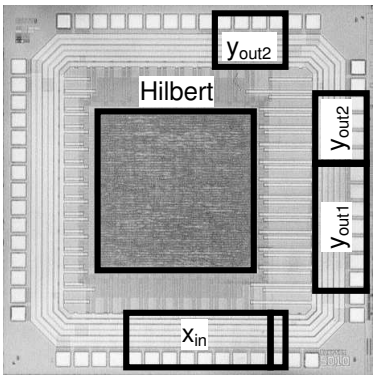


Figure 3. Microphotograph of the 31-tap FIR Hilbert transformer chip.

Table 1. FIR Hilbert transformer chip specifications.

Feature	Value
Technology	0.35 μm CMOS, 4-layer metal
Core size	0.86mm^2
Number of transistors	32988
Filter order	31taps
I/O word	8bits
Clock Frequency	71 MHz
Power dissipation	263 mW @ 70 MHz

and has less power dissipation after ASIC implementation.

4. Hilbert Transformer VLSI Implementation

The specifications of the 31-tap FIR Hilbert transformer are presented in Table 1 and a microphotograph is shown in Fig. 3.

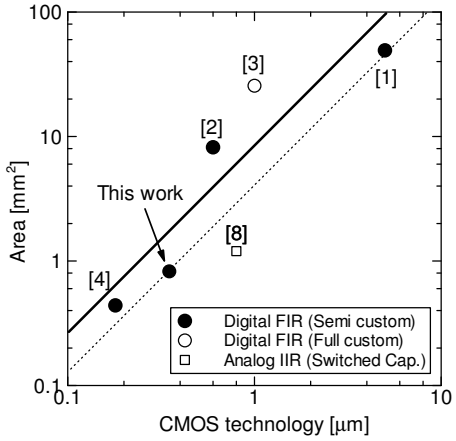
Trends regarding the chip area of a Hilbert transformer are summarized in Fig. 4(a). We can estimate a 47% reduction in the area compared with the earlier Hilbert transformer made using the same fabrication technology. Also, Fig. 4(b) shows the trends regarding the critical path time of a Hilbert transformer. From this figure, we can estimate a 24% reduction in the area compared with the earlier Hilbert transformer.

5. Conclusions

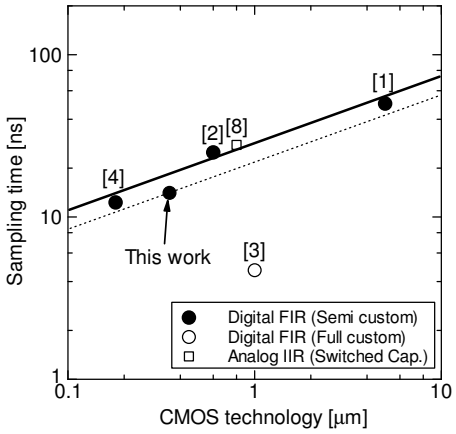
We have presented the design and implementation of a 31-tap FIR Hilbert transform digital filter chip. The architecture has been based on a computation sharing multiplier using vertical and horizontal common subexpression elimination techniques. The chip has been implemented by using a 0.35 μm CMOS process technology with the area of 0.86 mm^2. The chip has been a clock frequency of 71 MHz and a power consumption of 263 mW at 70 MHz.

Acknowledgment

The Hilbert transformer chip in this paper has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Co. Ltd. and Toppan Printing Co. Ltd.



(a)Relationship of area between CMOS technology.



(b)Relationship of sampling time between CMOS technology.

Figure 4. Technical roadmap of Hilbert transformer. The numbers in the brackets are references.

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