A Matched-Filterless Spread Spectrum Communication System

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Abstract: A new Spread Spectrum (SS) communication system is proposed in this paper. In the proposed system, by specially establishing the pilot signal channel which is used for capturing the synchronization, both of capture and hold operations are able to be realized only by the Delay Locked Loop (DLL) without using any matched filter in the receiving side. Not only the circuit scale of the receiver can be reduced by omitting the matched filter, but also the demodulation of directly amplitude-modulated SS wave becomes possible. The system operation was experimentally confirmed by using a circuit consisting of the discrete components.

1. Introduction

In the CDMA communication, it is indispensable to synchronize the spread code at the receiver side with that at the transmitter side. The synchronization capture and hold are necessary in the synchronous operation [1]. Conventionally, a matched filter using Surface Acoustic Wave (SAW) filer or Charge Coupled Device (CCD) filter has been used as the synchronization capture circuit. However, as the spread code length increases, the circuit becomes more complicated. Also because the delay stage is required by the bit number of the spread code, the circuit scale gets large.

To solve these problems, it is shown in this paper that synchronization can be realized only by the DLL without using the matched filter by positively utilizing the DLL by equipping different pilot channel with the information channel. In addition, in the proposed SS communication system, demodulation of directly amplitude-modulated signal that is impossible with the conventional method becomes possible.

2. A New Spread Spectrum Communication System

The proposed SS communication system is shown in Fig. 1. In the transmitter side (Fig. 1 (a)), the clock pulse which is output from a voltage controlled oscillator (VCO) is divided by four with a chip clock generator. The chip clock pulse is input to a PN code generator. The pilot signal is generated by multiplying direct current (DC) signal by the PN code which is generated by the PN code generator. The information signal is spread by multiplying the PN code which differs from the phase of the PN code used for generating the pilot signal by the information signal. Similarly, another information signal is spread by multiplying another information signal by the PN code which has the unused phase. Two or more PN codes, each phase of which is respectively different to another, are taken out of the PN generator by changing the tap to take out the PN code. Since the correlation value between PN codes is little value near zero, the spread signals do not interfere each other. Therefore, the pilot signal can be mixed with the spread information signals and be transmitted. As a example, it is shown in Fig. 1 that the spread signals of three channels are generated.

In the receiver side (Fig. 1 (b)), the synchronization is captured and held by using the pilot signal. The synchronous capture and hold are realized by using the DLL, the stepped waveform generator, the synchronization channel and the synchronization judgment circuit. In the receiver side, two same type PN code generators are required for the receiving pilot channel and demodulating the spread signals. The received PN code is generated in a method similar to the transmitter side. In Fig. 1, the PN codes have different phase by $-T_c/2$ and $T_c/2$ as against the reference PN code. Also, the PN codes are generated for the receiving pilot channel by using the chip clock pulse which has different phase by π [rad] as against the reference pulse. In the case of synchronization, by taking the received PN code (which equals the phase of transmitted PN code) out of each taps in PN generator at the receiver side and multiplying the PN code by the received spread signal, the spread information signal is despread and demodulated the original information signal. The synchronization judgment circuit judges the synchronization of the pilot signal. When the synchronization is achieved, the output voltage level from the stepped waveform generator is held. On the other hand, when the synchronization is not achieved, it is stepwise adjusted.

2.1 DLL (Delay Locked Loop)

The DLL circuit is shown in Fig.2. The DLL is originally used as the synchronization hold circuit. By correlating the received PN code which has different phase (i.e. $-T_c/2$ and $T_c/2$) and adding the correlation values, the control signal is generated (Fig. 3). The control signal is used for equalizing the frequency of the received PN code with that of the transmitted PN code [2].

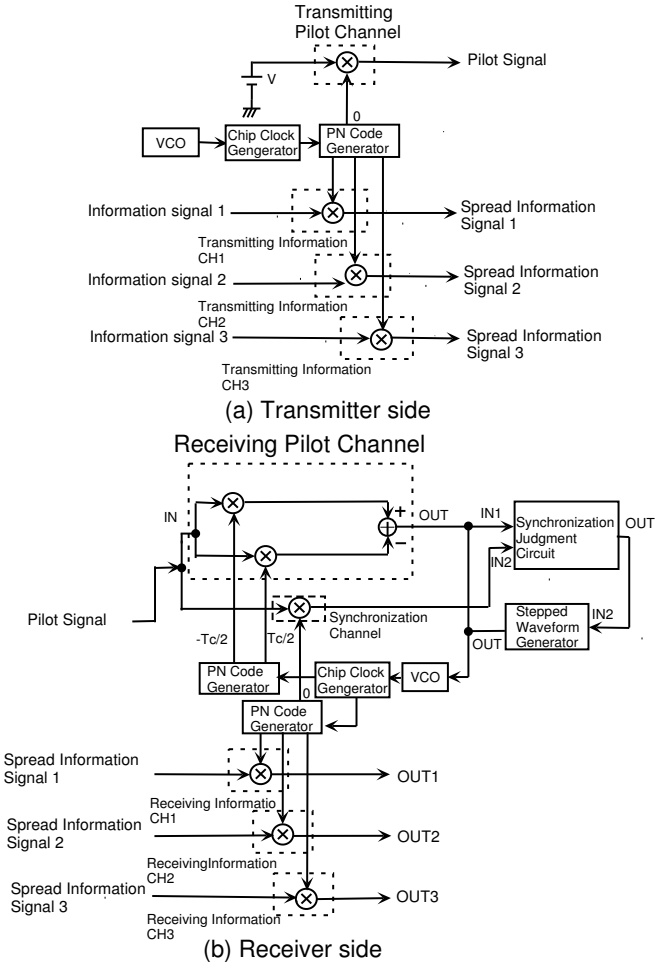

Figure 1. A new spread spectrum communication system.

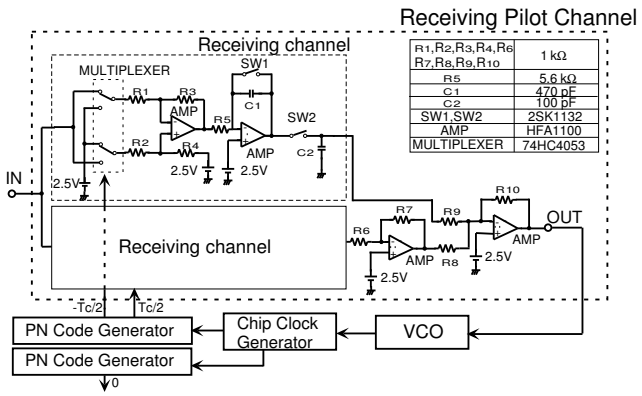

Figure 2. DLL circuit.

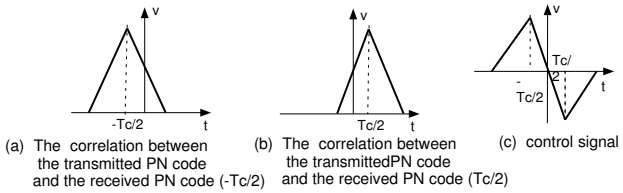

Figure 3. The correlation value between the transmitted side PN code and recieved side PN code and control signal.

However, if the synchronization is captured only by the DLL, the respective frequencies may equal in the state, which the phase of the received PN code differs from that of the transmitted PN code. Under such conditions, the phase of the received PN code is shifted by changing the frequency of the received PN code compulsively. As a result, the synchronization between the received PN code and the transmitted PN code is possible.

2.2 The Stteped Waveform Generator

The frequency of the received PN code must compulsively be changed by adding the special voltage to the VCO, when the synchronous capture can not be achieved only by the DLL. Accordingly, the stepped waveform voltage is input to the VCO until the synchronous capture is completed. The reason why the stepped waveform is required for the VCO is that we obtain the accurate correlation value between the received PN code and the transmitted PN code, by holding the voltage level for enough time before changing.

The stepped waveform generator is shown in Fig. 4. The stepped waveform generator is consisted of a 4bit-counter and a R-2R ladder type D/A converter. The clock pulse to drive the counter is input to IN_1. The clock pulse, which the clock frequency is 1kHz, is used. The output from the synchronization judgment circuit is input to IN_2. When the synchronous capture is not completed, since Low is input to IN_2, the counter continues to generate the stepped waveform. When the synchronous capture is completed, since $High$ is input to IN_2, the output voltage level from the stepped waveform generator is held. As a result, the synchronous capture is completed.

2.3 Synchronization Channel

The correlation value between the received PN code and the transmitted PN code is obtained by multiplying the pilot signal by the reference received PN code. When the synchronous capture is completed, the correlation value amounts to peak. Therefore, the output signal from the synchronization channel can be used as the signal of the synchronous judgment, thus it is input to the synchronization judgment circuit.

2.4 Synchronization Judgment Circuit

The synchronization judgment circuit is shown in Fig. 5. The synchronization judgment circuit is used for judging whether it is synchronized or not. The control signal is input to IN_1. The output signal from the synchronization channel is input to IN_2. At first, comparing between the control signal and the threshold voltages V_1, V_2 as shown in Fig. 5, the synchronous capture is determined. As a result, the output signal of AND1 (as shown in Fig. 5) is $High$ level. Secondly, we compare the output signal of AND1 with that of AMP3. When both of the generated two signals amount to $High$, it is judged that the synchronous capture is completed. Finally, the output voltage level from the stepped waveform generator is held by

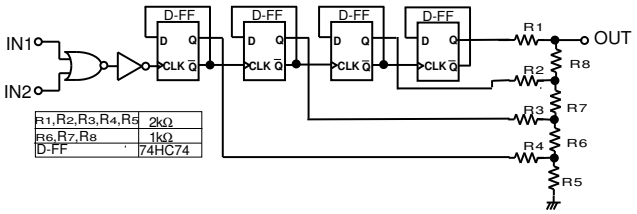

Figure 4. The stteped waveform generator.

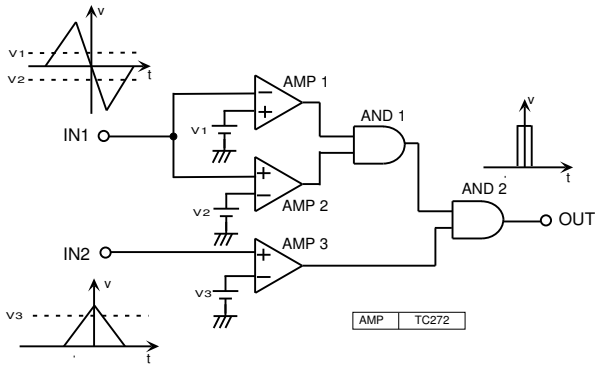

Figure 5. The synchronization judgment circuit.

inputting the signal to the counter.

3. Experimental Results

In order to confirm that the proposed SS system can perfectly operate, we conducted the experimental tests by using the discrete conponents. Table 1 summarizes the experimental conditions of the proposed SS system.

In Fig. 6, both of the PN code signals in the transmitter side and receiver side are shown, which are in the synchronization. As recognized from Fig. 6, it is confirmed that the frequency and phase of the PN code signal in the transmitter side meet with those of the PN code in the receiver side. In Fig.7, the transmitted base-band 1 kHz signal and the received signal are shown. As you can see from Fig. 7, it is found that the transmitted base-band signal is perfectly demodulated to the original base-band. In Fig.8, the spread pulse width modulated (PWM) base-band signal and the received base-band signal are shown. As recognized from Fig.8, since the spread PWM signal become as a noise, highly confidential communication is conducted by the transmitter. Furthermore, the received base-band signal is perfectly demodulated to the original signal. Figure9 depicts the received base-band 1kHz and 2kHz signals with two information channels. It is confirmed that the received base-band signals is perfectly demodulated

Table 1. Experimental conditions.

Name	Value
Chip clock	5.5 [MHz]
Base band signal 1	1 [kHz], 2.0 [V_{pp}], sine wave
Base band signal 2	2 [kHz], 2.0 [V_{pp}], sine wave

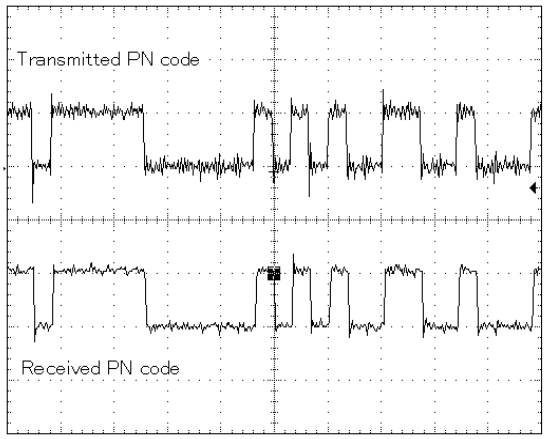

Figure 6. The transmitted/recieved side PN code in synchronization. Vertical scale:5V/div. Horizantal scale: 500ns/div.

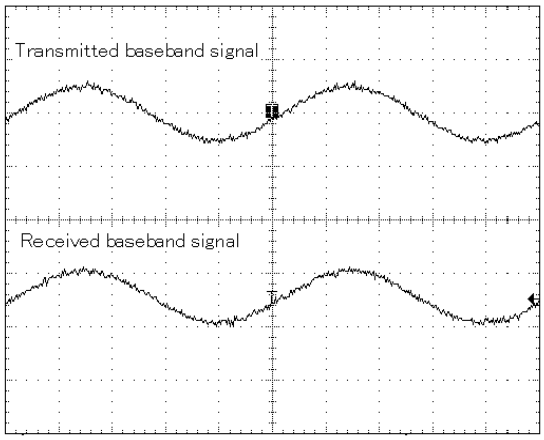

Figure 7. The transmitted/recieved base-band signal waveform. Vertical scale:2V/div. Horizantal scale:200μs/div.

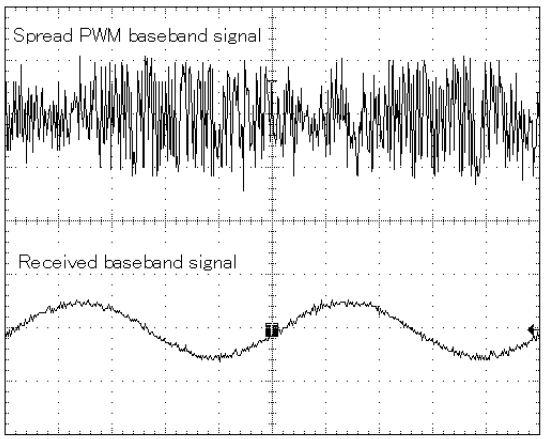

Figure 8. Spread PWM base-band signal waveform and received base-band signal waveform. Vertical scale: 2V/div. Horizontal scale: 200μs/div.

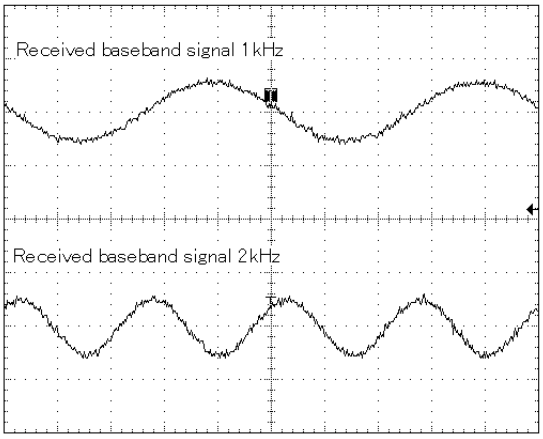

Figure 9. Received 1kHz and 2kHz base-band signal waveforms. Vertical scale: 2V/div. Horizontal scale: 200μs/div.

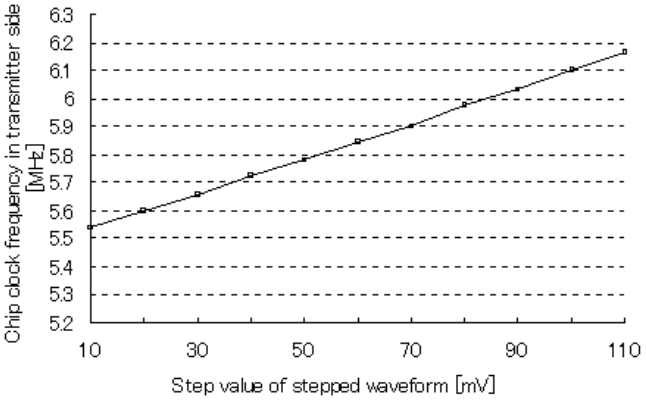

Figure 10. The relations between the step value of the stepped waveform and the chip clock frequency in transmitter side, which is able to synchronize.

without influencing each signal. In Fig.10, the relations between the step value of the stepped waveform and the chip clock frequency in transmitter side, which is able to synchronize, are shown. When the step value is 110 mV, if the chip clock frequency in transmitter side is from 5.5 MHz to 6.15 MHz, the proposed system enables the synchronization between the transmitted PN code and the received PN code. However, when the step value is more than 110mV, it is impossible that the system is to capture the synchronization. Because the change of the chip clock frequency in the receiver side is too large; that is we cannot obtain the control signal which is required for synchronizing.

4. Conclusions

In the paper, a novel Spread Spectrum Communication System has been proposed. The system does not need so-called matched filter as SAW filter or CCD filter for the synchronous capture and hold operation. Therefore, the complexity of the SS system has been decreased although the pilot channel is added for the synchronization. In the experimentation, the new SS system has been built by using discrete components. In the system, as the base-band signal, 1kHz and 2kHz sine waves were used and spread with 5.5 MHz chip clock PN code. The spread signal has been despread and the original base-band signal was obtained in the excellent state. In the case of using two information channels, two base-band signals were perfectly demodulated without influencing each signal. Moreover, highly confidential communication was enabled by transmitting PWM base-band signal. In addition, as a result of setting the step value of stepped waveform appropriately, the system was able to adjust to the change of chip clock frequency in transmitter side. It has been confirmed that the synchronous capture and hold method proposed in the paper is available for Spread Spectrum Communication System.

References

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