

Hilbert Transformer Design Using CSD FIR Filter

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Abstract: This paper describes the design of Canonic Signed-Digit (CSD) expression Hilbert Transformer (HT). The feature is algorithm of the direct-form FIR filter applied to HT, resulting in reduction of the number of the used adders. The number of the adders and delays in the proposed HT is compared with that in the conventional Hawley's HT. When the quantized coefficients are given by an 8-digit CSD code with 2 nonzero digits, the numbers of the required adders and delays are found to be reduced by 87.7%, and 83.9% respectively.

1. Introduction

Single Side Band (SSB) communication is widely used in the fields of Data communication, Wireless and Cellular communication, Ham radio communication, etc. Hilbert Transformer (HT) is one of the most important circuits which are used in synthesizing or demodulating SSB wave by the phasing method. This method needs to strictly shift the phase of signal by 90 degrees over wide range frequency. HT can be composed of either analog [1] or digital filter [2]; however, in recent years, it shows the tendency to use the digital filter along with the popularization of the digitization.

FIR filter can be realized by doing Multiply and Accumulate (MAC) operation. Since the multiplier has many gates, FIR filter with many coefficients becomes a large scale of circuit. However, it is known that the FIR filter can be composed only of the adder by making the coefficient to be the Canonic Signed Digit (CSD) expression. Hawley et al. [2] has produced the VLSI of the CSD expression HT. However, since high speed was required to Hawley's HT, it was realized by the folded direct-form transpose FIR filter. As a result, Hawley's HT has become a large scale of circuit. On the other hand, Suzuki et al. [3] has proposed the algorithm of the direct-form FIR filter design that can be constituted in the least number of adders using CSD.

2. Proposed HT

The coefficient of the direct-form FIR filter [3] is shown in Fig.1. The labels of the coefficient and of the adder are given by

$$\begin{aligned} \text{N:even} \quad & i=0, \dots, \frac{N}{2}-1 \\ & E(a_i) = x[i] + x[N-1-i] \\ & C(a_i) = \text{CSD}(h_i) \end{aligned} \quad (1)$$

and

$$\begin{aligned} \text{N:odd} \quad & i=0, \dots, k-1, k = \frac{N-1}{2} \\ & E(a_i) = x[i] + x[N-1-i], E(a_k) = x[k] \\ & C(a_i) = \text{CSD}(h_i), C(a_k) = \text{CSD}(h_k) \end{aligned} \quad (2)$$

(N is the number of coefficients)

	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	
a_0	0	0	$\bar{1}$	0	1	$E(a_0) = x[0] + x[6]$
a_1	0	0	1	0	$\bar{1}$	$E(a_1) = x[1] + x[5]$
a_2	0	1	0	0	1	$E(a_2) = x[2] + x[4]$
a_3	1	0	$\bar{1}$	0	$\bar{1}$	$E(a_3) = x[3]$

$C(a_2)$

Set A

Fig.1. Table of coefficient and ensemble (N=7).

Note that, $\bar{1} = -1$. At first, correlation of each other coefficient digit pattern is investigated. When there is the correlation, either digit pattern is shifted only to the horizontal direction. As a result, it is considered that the moved digit is a common digit pattern, and the number of adders decreases. Suzuki has succeeded in reduction of adders using this procedure. The flow chart which shows this procedure is shown in Fig.2.

Next, we consider that Suzuki's algorithm applies to HT. When HT is as the center-symmetry bandpass filter, the coefficient of bandpass filter has interleaved zero's. Therefore, the number of adders decreases because the odd label $E(a_i)$ is set to 0. HT is composed of either even or odd number of taps. However, in the odd case, the number of adders is decreased because coefficient of a center tap is set to $C(a_i) = \text{CSD}(h_i) = 0$.

Hence, when HT is designed with the odd tap and center-symmetry bandpass filter, the number of adders becomes the minimum. A label (2) is reduced to:

$$\begin{aligned} & E(a_i) = x[i] - x[N-1-i] \\ & C(a_i) = \text{CSD}(h_i) \end{aligned} \quad (3)$$

where $i=0, 2, 4, \dots, 2m, \dots, k-1$, and m is integer number. The 2nd term of label $E(a_i)$ is set to negative value because the tap of HT is odd-symmetry. The coefficient table of HT is shown in Fig.3. Operation of the coefficient digit pattern is possible in the same procedure as the flow chart shown in Fig.2.

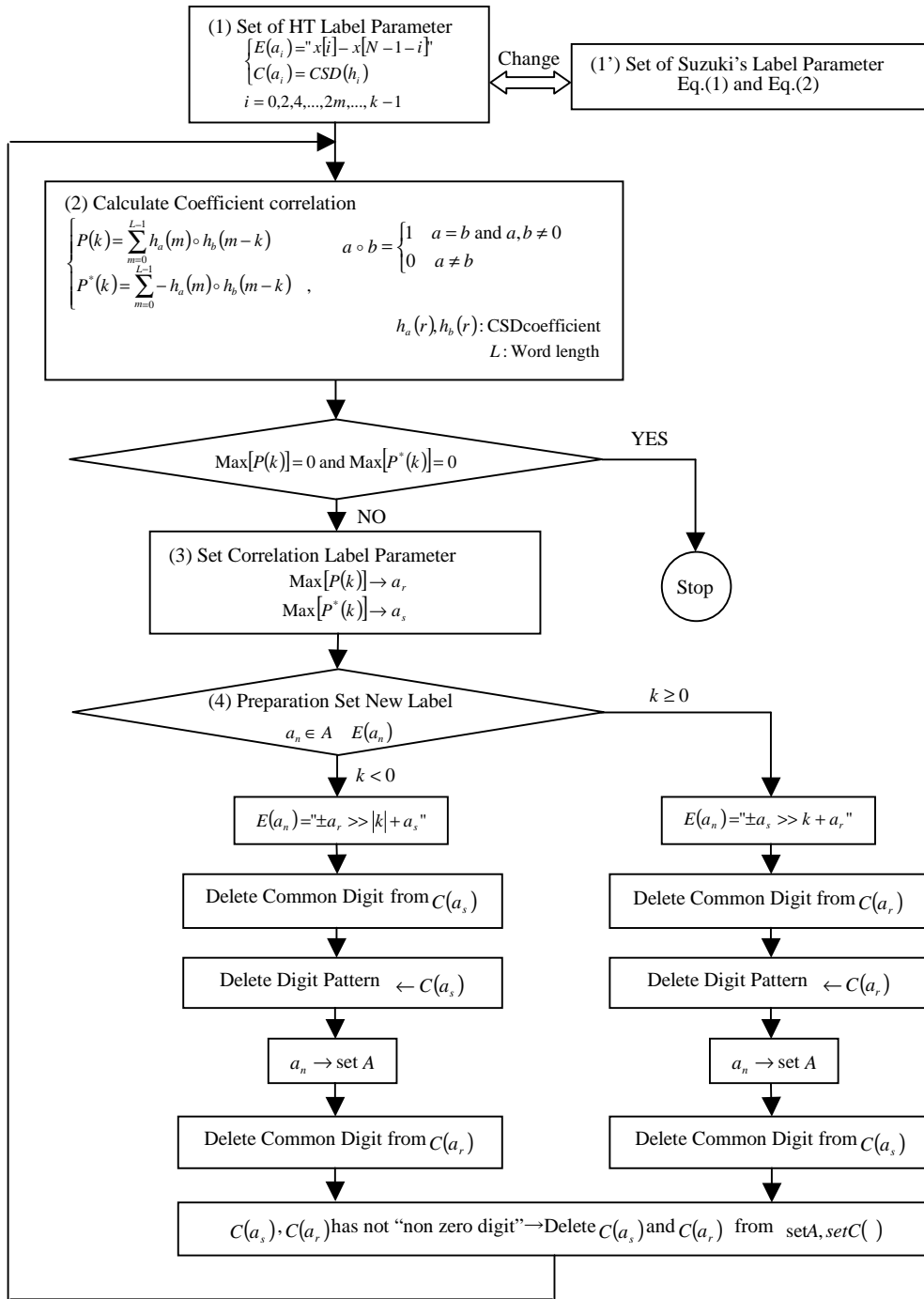


Fig.2. Flow chart of Algorithm.

	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	
a_0	0	0	$\bar{1}$	0	1	$E(a_0) = x[0] - x[6]$ $E(a_2) = x[2] - x[4]$
a_2	0	0	1	0	$\bar{1}$	

$C(a_s)$

Set A

Fig.3. Table of the HT coefficient and ensemble (N=7).

3. Simulation

Example 1: Consider a parameter with Table 1. The Frequency response is shown in Fig.4 and the signal flow is shown in Fig.5.

Table 1 Design parameter for 15-tap HT		
Taps 15	Coefficient words 8bit	Non-zero Bit 2bit
Filter Coefficients		
$H = (-1,0,-12,0,-7,0,64,0,-64,0,7,0,12,0,1) \times 2^{-7}$		

From a Fig.5, we find that the 15-tap FIR-HT can be realized by using only 8 adders, and only 14 delays. This filter has the normalized passband [0.15,0.35].

Example 2: We next consider an example with a wider passband. New parameter is set to Table 2. The Amplitude-Frequency response is shown in Fig.6. and the signal flow is shown in Fig.7.

Table 2 Design parameter for 31-tap HT		
Taps 31	Coefficient words 8bit	Non-zero Bit 2bit
Filter Coefficients		
$H = (-4,0,-3,0,-2,0,-1,0,3,0,9,0,20,0,80,0,80,0,-20,0,-9,0,-3,0,1,0,2,0,3,0,4) \times 2^{-7}$		

From a Fig.7, when the number of taps changes from N=15 to N=31, 23 adders and 30 delays are required. This filter has the normalized passband [0.05,0.45].

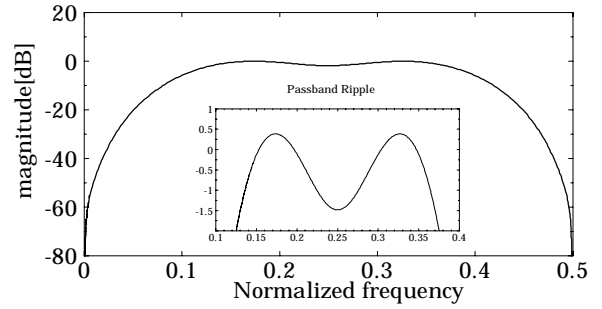


Fig.4. Frequency response for 15-tap HT Filter.

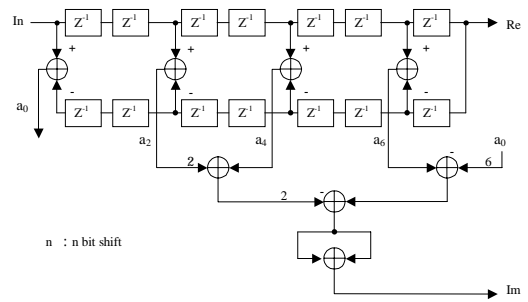


Fig.5. Signal Flow for 15-tap HT Filter.

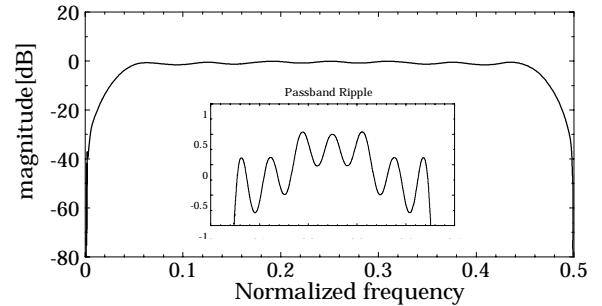


Fig.6. Frequency response for 31-tap HT Filter.

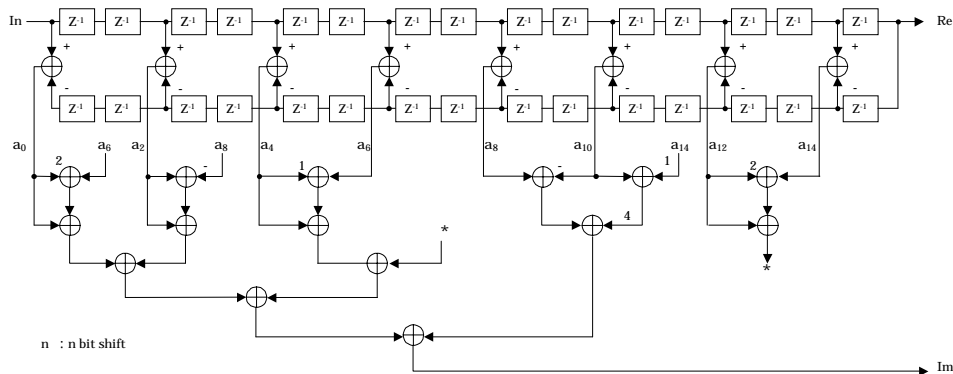


Fig.7. Signal Flow for 31-tap HT Filter.

4. Required Adders and Delays

Hawley has constituted HT using the block which consists of an adder and delay using CSD expression shown in Fig.8. Since this method has not been shared of a coefficient digit pattern, the number of adders cannot be restricted.

Comparing the proposed HT with Hawley's HT in Example.2 is shown in Table 3. By using the proposed method, the number of required adders and delays are reduced by 87.7%, and 83.9%, respectively.

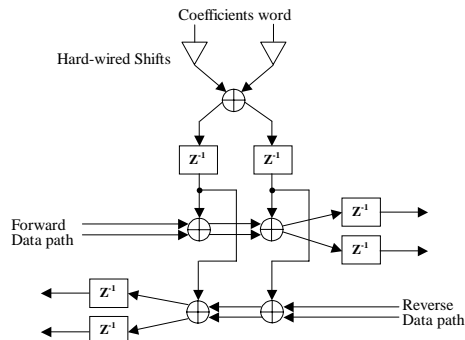


Fig.8. Structure of Hawley's HT filter tap.

Table 3 Comparison for adders and delays

	(A)Hawley	(B)Proposed	$\left(1 - \frac{B}{A}\right)$ [%]
ADDER	187	23	87.7
DELAY	186	30	83.9

5. Conclusion

Using CSD expression, we have designed direct-form HT composed of the least number of adders. The proposed HT has been compared with Hawley's HT. As a result, the numbers of the required adders and delays are reduced by 87.7%, and 83.9%, respectively.

In this paper, non-zero digit is restricted to 2 bits, and coefficient word length is restricted to 8 bits. Since those are not always optimum value, it is possible that the number of adders decreases more in the case of other bit combination. In addition, retiming of the circuit cannot be performed because the delay of real part and imaginary part is shared. Thus there are possibilities that the critical path length becomes long. In future, it is necessary to verify these problems.

References

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