Low-Power Adiabatic SRAM

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Abstract—**This paper presents a new adiabatic static random access memory (SRAM). The proposed adiabatic SRAM uses two trapezoidal-wave pulses and resembles behavior of static CMOS 4T-SRAM. The elementary cell structure of proposed SRAM consists of two high load resistors which is constructed of PMOS, a cross-coupled NMOS pair and NMOS switch which is necessary to restrict short circuit current. From the simulation results, we show that the energy consumption of the proposed circuit is lower than that of conventional SRAM.**

I. INTRODUCTION

In the design of low-power VLSI processor, adiabatic (or energy recovery) logic and memory show great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{dd}^2/2$. The adiabatic logics [1]–[10] and the adiabatic memories [11]–[16] are a very attractive solution for low power consumption. The adiabatic memories are categorized as follows: static cell types [11], [15], [16]; latch types [12], [13]; and dynamic type [14]. In current consumer processor, the use of SRAM L2 cache tends to drastically increase the processor die size and hence reducing power dissipation in SRAM will remain a critical issue.

In this paper, we propose a novel low-power adiabatic SRAM with controlled sudden current flow. The proposed circuit which is driven by two trapezoidal-wave pulses can be directly converted from the conventional SRAM circuits, without drastically increasing the circuit area. Through the computer simulation we show that the energy consumption of the proposed circuit is drastically lower than that of conventional logic circuit.

II. ADIABATIC OPERATION IN LSI

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown like in Fig. 1, where V_{dd} becomes a DC voltage while the inverter works as CMOS static mode. When the logic level in the system is "1", there is a sudden flow current through R_p, where R_p is equivalent resistance of PMOS pull-up network.

A charge $Q = CV_{dd}$ is delivered to the load and the energy which the supply applies is $E_{supply} = QV_{dd} = CV_{dd}^2$, where V_{dd} is a DC power supply voltage. The energy stored into the load C is a half of the supplied energy: $E_{stored} = \frac{1}{2}CV_{dd}^2$. The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle: $E_{total} = E_{charge} + E_{discharge} = \frac{1}{2}CV_{dd}^2 + \frac{1}{2}CV_{dd}^2 = CV_{dd}^2$. If the logic is driven by a certain frequency $f (= 1/T)$, where T is the period of the signal, then the power of the CMOS gate is determined as: $P_{total} = \frac{E_{total}}{T} = CV_{dd}^2 f$.

The main idea in an adiabatic switching shown in Fig. 1 is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the $Q = CV_{dd}$ charge during the time period ΔT, the energy dissipation in the channel resistance R_p (or R_n) is given by

$$
\begin{aligned}
E_{Dias} &= \xi P \Delta T \\
&= \xi I^2 R_p \Delta T \\
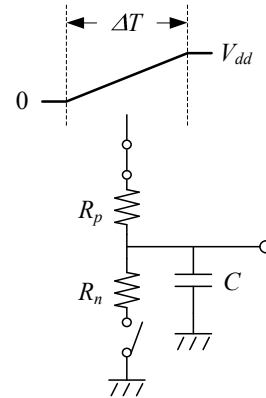&= \xi \left(\frac{CV_{dd}}{\Delta T} \right)^2 R_p \Delta T,
\end{aligned} \tag{1}
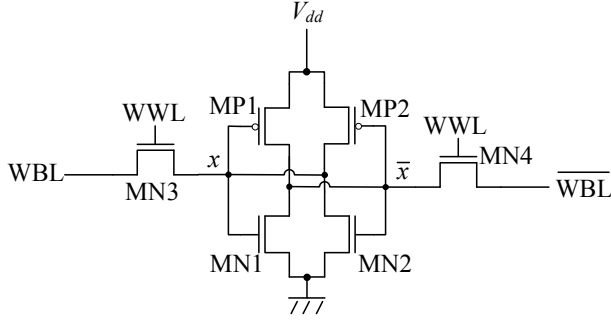$$

Fig. 1. RC tree model of adiabatic switching.

Fig. 2.   Conventional CMOS 6T-SRAM.

Fig. 3.   Input waveforms of conventional 6T-SRAM with adiabatic mode.

where ξ is a shape factor which depends on the shape of the clock edges [17]. It takes on the minimum value $\xi_{min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period ΔT is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [1].

III. PROPOSED ADIABATIC SRAM

A. Conventional CMOS SRAM

The conventional 6T-SRAM design is shown in Fig. 2. The elementary cell of 6T-SRAM is CMOS inverter latch, and their output node x and $\overline{x}$ hold the input data. When write line WWL becomes HIGH state, the SRAM cell is possible to be the write mode. If the operation of conventional 6T-SRAM is changed to quasi-adiabatic mode, the input waveforms (WWL, WBL, and $\overline{\text{WBL}}$) use the trapezoidal pulse as shown in Fig. 3. Figure 4 depicts the output waveforms and its power dissipation of 6T-SRAM with adiabatic mode. In this simulation, we use 0.18 μm CMOS standard process where the size of NMOS is $W/L = 0.60 \ \mu$m/0.18 μm. This figure is shown that the conventional 6T-SRAM can correctly operate, but the energy dissipation drastically increase while write-state transition.

B. Proposed SRAM

The proposed SRAM is shown in Fig. 5, and its input timing is shown in Fig. 6. The elementary cell of proposed circuit consists of two high load resistors which is constructed of PMOS (MP1 and MP2), and a cross-coupled NMOS pair (MN1 and MN2). In order to reduce the energy dissipation in the elementary cell, the PMOS having off-leak current is used. Using the PMOS as a high resistor the cell area can be small compared with the conventional 4T-SRAM using poly resistor. NMOS switch (MN3) is necessary to restrict a short circuit current when the data is written in the elementary cell. In the proposed circuit, decreasing signal voltage on the write (or read) line is limited by transmission gate; however normal NMOS switch is better from the viewpoint of cell area if voltage drop is no problem.
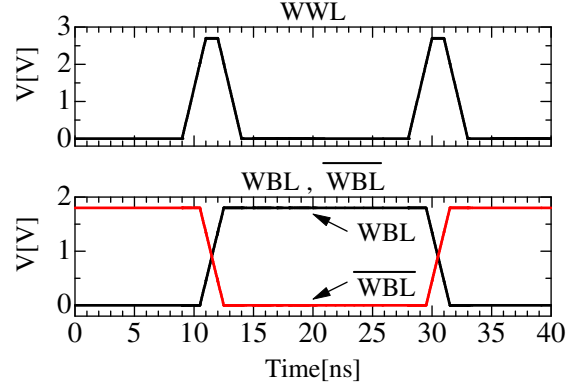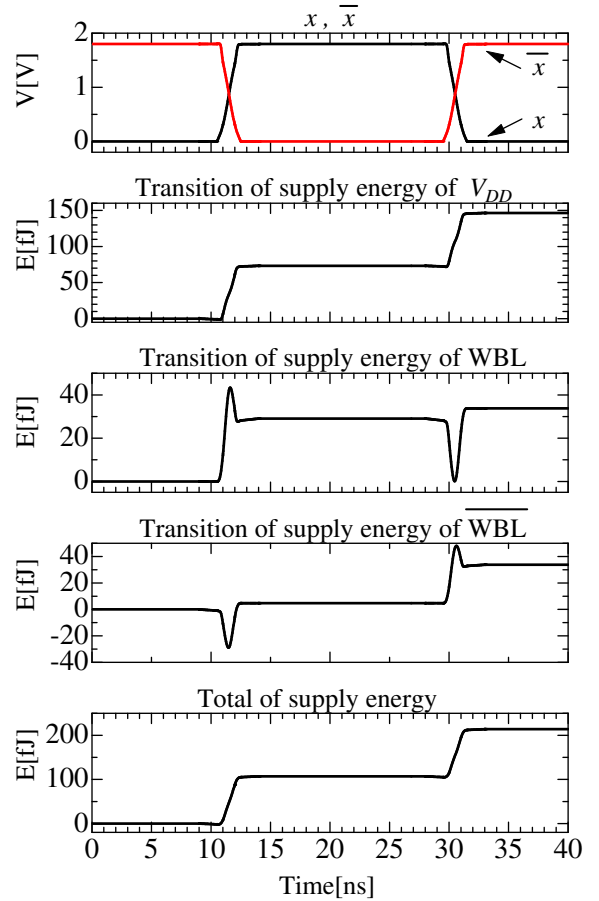

Fig. 4.   Output waveforms and energy dissipation transition of conventional 6T-SRAM with adiabatic mode.

The write mode of the proposed SRAM is as following. At first phase, when WWL is High and $\overline{\text{WWL}}$ is Low level, MOS transistors: MN4, MN5, MP3, and MP4 are ON. Hence, the node x and $\overline{x}$ is possible to change the write-mode, and then MN3 is OFF in order to reduce the energy dissipation in the elementary cell. In second phase, adiabatic signal line
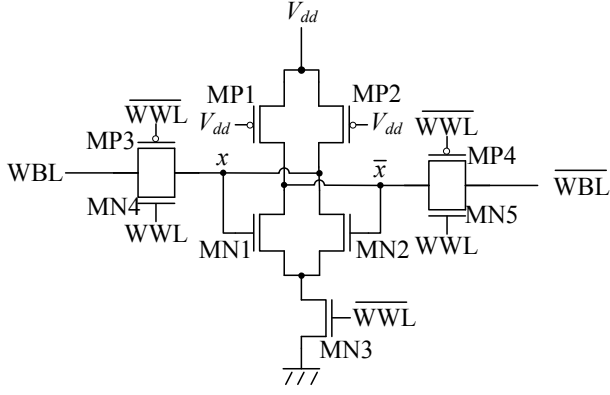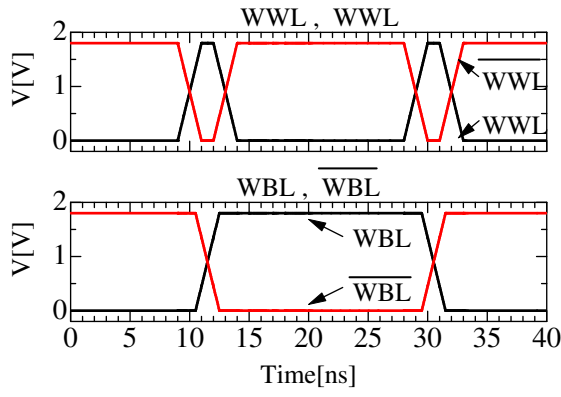
Fig. 5. Proposed SRAM.

Fig. 6. Input waveforms of proposed SRAM.

Fig. 7. Output waveforms and energy dissipation transition of proposed SRAM.

WBL, and $\overline{\text{WBL}}$ are on-state, and then the data write on x and $\bar{x}$. Finally, when WWL and $\overline{\text{WWL}}$ are Low and High state respectively, MOS transistors: MN4, MN5, MP3, MP4 become all OFF, and then MN3 becomes ON. As a result, data is hold state in the elementary cell.

IV. SIMULATION RESULTS

The conventional SRAMs and the proposed SRAM are tested by SPICE simulation using a 0.18 μm standard CMOS process technology. The parameters of the proposed circuit and simulation conditions are summarized in Table I. To evaluate the power savings in the circuits, we compute the energy consumption E, which is defined as follows:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{p_i} I_{p_i}) \right) dt, \qquad (2)$$

where $T_s (= 1/f_s)$ is the period of the primary input signal, V_p is the supply voltage, I_p is the supply current, and i is a number of supply source. Therefore, E is equal to the net energy flowing into the circuit from the supply line. As discussed in [10], energy transfers between the controlling signals and the controlled signals. Within a cycle (charging
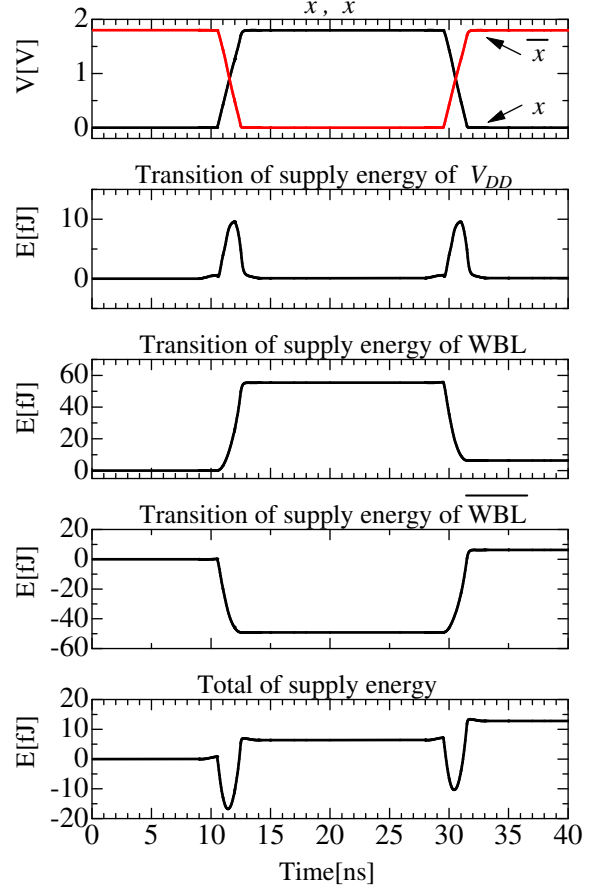
and discharging), energy flows into the circuit and is recovered back from it. The level difference of E in two (or more) consecutive cycles reflects the energy loss in a full cycle. The effect of energy transfers between the controlling and the controlled signals leads to the energy transferring from one phase of power supply to another. Therefore, we have to compute the "Net energy" by summing up the energy in power supply lines.

Figures 7 show the output waveforms and the energy dissipation transition of proposed SRAM. From these figure the output is correctly hold data after writing "1" and "0," and the power dissipation is lower, especially at the write-mode.

Table II summarizes the energy dissipation values. From this table, we find that energy dissipation of proposed is drastically

TABLE II
COMPARISON OF ENERGY DISSIPATION BETWEEN CONVENTIONAL AND
ADIABATIC SRAM.

	Energy [fJ]
CMOS	107.08
Adiabatic [15]	93.58
Proposed Adiabatic	6.40

reduced compared to those of the conventional 6T-SRAM and adiabatic-SRAM [15].

V. CONCLUSION

In this paper, we have presented an adiabatic SRAM. The proposed SRAM has used two trapezoidal-wave pulses and has been controlled switching current flow. Our simulation result with the proposed circuit has indicated a factor of 14 over reductions in energy consumption.

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