Memristor 1T-SRAM with Adiabatic Driving

Yasuhiro Takahashi, Yuki Urata, and Toshikazu Sekine
Department of Electrical and Electronic Engineering,
Gifu University, Japan
1-1 Yanagido, Gifu-shi, 501-1193
Email: {yasut, seki}e@gifu-u.ac.jp

Nazrul Anuar Nayan
Department of Electrical, Electronic and Systems Engineering,
National University of Malaysia,
43600 UKM Bangi, Selangor, Malaysia
Email: naz@eng.ukm.my

Michio Yokoyama
Department of Bio-system Engineering,
Yamagata University, Japan
4-3-16 Jonan, Yonezawa-shi, 992-8510
Email: yoko@yz.yamagata-u.ac.jp

Abstract—This paper proposes a novel adiabatic static random access memory (SRAM) using memristor. The proposed SRAM which is a sinusoidal driving consists of one NMOS transistor and one memristor (i.e. 1T1M type). The proposed SRAM also is driven by an optimal voltage resulting in a decrease of energy dissipation. From SPICE simulation results, we show that the energy dissipation of proposed 1T1M-SRAM with a sinusoidal driving voltage is lower than that of the conventional pseudo-SRAM called IT1C, and the proposed circuit is especially effective against reducing power consumption at logic Hi-state.

Keywords—SRAM, pseudo SRAM, memristor, adiabatic, low power

I. INTRODUCTION

In 1971, Chua has pointed out the existence of the fourth passive component called memristor [1]. This element is defined by a nonlinear relationship between the charge and the magnetic flux, and therefore it can be used as a nonlinear resistor with memory. After 37 years, the first experimental realization of memristor has demonstrated in a solid-state thin film two terminal device by HP Labs [2]. The memristive effect has achieved by moving the doping front along the device. This discovery has attracted a great attention. Many potential applications are reported, e.g., the memories for low cost technology [3], [4], programmable logic [5], and reconfigurable logic [6].

The adiabatic logics [7]– [15] and the adiabatic memories [16]– [21] are very attractive solution for low power consumption but the papers have proposed that the conventional memory structures have used – e.g. 6 transistor (6T) based, 8T, inverted-latch, and Flip-Flops (FF), and whereby there is positive need for small-size and low-power adiabatic memory for the next-generation.

In this paper, we present a new adiabatic pseudo-SRAM using a memristor. The proposed SRAM builds on a single NMOS transistor and one memristor, and hence it is like DRAM. The proposed SRAM also is driven by an optimal sinusoidal voltage resulting in a decrease of energy dissipation. The rest of the paper is organized as follows. Section II summarizes the most important properties of the adiabatic logic. The properties of memristor is briefly described in Section III. The proposed memristor based 1T-SRAM is presented and is evaluated in Section IV. Finally the conclusions are given in Section V.

II. ADIABATIC LOGIC

A. Conventional vis-a-vis Adiabatic Switching

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1(a). When the logic level in the system is “1”, there is a sudden flow current through R, where R is equivalent resistance of PMOS pull-up network. A charge Q = CVdd is delivered to the load and the energy which the supply applies is $E_s = QV_{dd} = CV_{dd}^2$, where $V_{dd}$ is a DC power supply voltage. The energy stored into the load C is a half of the supplied energy:

$$E_{stored} = \frac{1}{2} CV_{dd}^2.$$  (1)

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{grnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$E_{total} = E_{charge} + E_{discharge} = \frac{1}{2} CV_{dd}^2 + \frac{1}{2} CV_{dd}^2 = CV_{dd}^2.$$  (2)

If the logic is driven by a certain frequency $f (= 1/T)$, where $T$ is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T} = CV_{dd}^2 f.$$  (3)

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word “adiabatic” (Greek
adiabatos, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. The main idea in the adiabatic switching shown in Fig. 1(b) is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the charge during the time period \( \Delta T \), the energy dissipation in the channel resistance \( R \) is given by

\[
E_{\text{diss}} = \xi P \Delta T \equiv \xi T^2 R \Delta T = \xi \left( \frac{CV_{dd}}{\Delta T} \right)^2 R \Delta T, \tag{4}
\]

where \( \xi \) is considered as the average of the current flowing to \( C \), and \( \xi \) is a shape factor which depends on the shape of the clock edges [22]. It takes on the minimum value \( \xi_{\text{min}} = 1 \) if the charge of the load capacitor is DC modulated. For a sinusoidal current, \( \xi = \pi^2/8 = 1.23 \). The above equation indicates that when the charging period \( \Delta T \) is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [7].

III. MEMRISTOR

A. Theory

In [1], a charge-controlled memristor as shown in Fig. 2 is defined as a two-terminal element in which the magnetic flux \( \varphi \) between the terminals is a function of the amount of electric charge \( q \). The voltage \( v(t) \) across the memristor is given by

\[
v(t) = M(q(t))i(t) \tag{5}
\]

where \( M(q(t)) = d\varphi(q(t))/dq(t) \) is a memristance. The memristance becomes constant which acts like resistance while in the linear case. However, \( \varphi - q \) relation is non-linear whereby the element is referred to as memristance which can be charge-controlled.

B. SPICE model of HP’s memristor

In [2] the authors have realized a memristor which consists of a thin layer of TiO\(_2\) and a second oxygen deficient layer of TiO\(_{2-x}\) sandwiched between two Pt nanowires. The voltage-current relationship of this memristor is modeled as:

\[
M(q(t)) = R_{\text{ON}} \frac{w(t)}{L} + R_{\text{OFF}} \left(1 - \frac{w(t)}{L}\right)i(t), \tag{6}
\]

where \( R_{\text{ON}} \) is the resistance for completely doped memristor, \( R_{\text{OFF}} \) is the resistance for the undoped region and also \( L \) is the TiO\(_2\) film thickness. The width of the doped region \( w(t) \) is given by

\[
\frac{dx(t)}{dt} = \mu_e \frac{R_{\text{ON}}}{L^2} i(t), \tag{7}
\]

where \( \mu_e \) represents the average dopant mobility.

Lehtonen and Laiho have solved the differential equation (7) by using injective function [23] and obtained SPICE model of HP’s memristor. Using their SPICE parameters memristance is calculated as following:

\[
M(q(t)) = \frac{d\varphi(q(t))}{dq(t)} = 25 \left[1 - (2q(t) - 1)^2\right]. \tag{8}
\]

Figure 3 shows the voltage-current relationship (I-V curve) of HP’s memristor when above condition is provided. In this work, SPICE model of memristor is used as shown in this figure.

IV. PROPOSED 1T-SRAM

A. Structure

Figure 4 is the basic structure for a memristor NMOS storage cell [4]. This storage cell is a similar ITIC circuit using FRAM [24] or capacitor [25]. Figure 5 depicts timing diagram for writing “1” and “0” operation which has described in [4]. For writing a logic “1,” the memristor receives a positive bias to maintain an ON state. This is equal to the memristor being programmed as a logic HI. To program a “0” a reverse bias is applied to the memristor, which makes the memristor resistance high. This is comparable to logic LOW being programmed.

The proposed 1T-SRAM structure is the same as memristor NMOS storage. However, timing diagram is clearly distinct in that the threshold voltage of NMOS transistor is considered. Figure 6(a) illustrates the proposed timing diagram in order to achieve optimum output signal and low-power dissipation. The on-state voltage drop of the NMOS causes decreasing output voltage \( V_{\text{out}} \), hence the voltage for driving signal (DS) should set as: \( V_{\text{DD}} + V_t \), where \( V_{\text{DD}} \) and \( V_t \) are power supply voltage and threshold voltage for NMOS transistor, respectively. As a result voltage bias level \( \text{VL} \) is set to \( V_{\text{DD}} + V_t/2 \). To reduce the power consumption of memory, top level for writing signal (WS) is adjusted to \( V_{\text{DD}} \) because switching losses increase when the gate voltage is driven beyond \( V_{\text{DD}} \). When the proposed SRAM is changed to adiabatic mode, DS waveform is replaced pulse by trapezoidal (or sinusoidal) as shown in Fig. 6(b).

B. Comparison and Evaluation

To evaluate the operation and the energy dissipation of memory, the 1T-based adiabatic SRAM was tested by SPICE simulation using an 0.18 \( \mu \)m, 1.8 V CMOS standard process technology. The transistor size \( W/L \) is 0.6 \( \mu \)m/0.18 \( \mu \)m for the NMOS transistor.

The SPICE simulation results obtained for the 1T-SRAM are shown in Fig. 7. Figure 7(a) demonstrates the input signals: pulse, trapezoidal and sinusoidal, the write-bit signal: WS; Figure 7(b) shows the output waveform. From these figure
the output data is correctly hold-state after writing “1” and “0.”

Table I summarizes the energy dissipation values of each function. As can be seen from this table, the energy dissipation of proposed 1T-SRAM with sinusoidal wave is much smaller than that of 1T-SRAM with conventional pulse driving.

Figure 8 shows the comparison of energy dissipation between proposed (1T1M) SRAM and conventional (1T1C). The capacitor size of 1T1C is set to 100 fF, if the capacitor is fabricated using poly insulator poly (PIP). This figure shows that energy dissipation of 1T1M is drastically decreased compared to the 1T1C, especially at “1” writing mode.

V. CONCLUSION

In this paper we have presented a new adiabatic memory which is consists of 1T1M. The simulation results have shown that 1T1M driving sinusoidal wave has 17.5 fJ when each “1” and “0” write, and also the energy dissipation of proposed memory is smaller than that of conventional 1T1C memory cell.

REFERENCES

Fig. 3. I-V curve of HP’s memristor.

Fig. 4. Memristor-NMOS storage cell.

Fig. 5. Timing diagram of memristor-NMOS storage cell. (a) Program “LOW” resistance “1.” (b) Program “HI” resistance “0.”

Fig. 6. Proposed timing diagram. (a) D/S, WS and VL with optimal voltage. (b) adiabatic mode.

(a) Voltage timing: WS and DS (pulse, tra. and sin. wave).

(b) Output waveform.

Fig. 7. Input/output waveforms of 1T-SRAM using memristor.

Fig. 8. Comparison of energy dissipation between proposed 1T1M-SRAM and conventional 1T1C.

TABLE I
COMPARISON OF ENERGY DISSIPATION DEPEND ON THE DIFFERENCE IN INPUT WAVEFORM

<table>
<thead>
<tr>
<th>Waveform</th>
<th>Energy dissipation [fJ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td>34.3 (100%)</td>
</tr>
<tr>
<td>Trapezoidal</td>
<td>33.3 (97%)</td>
</tr>
<tr>
<td>Sinusoidal</td>
<td>17.5 (51%)</td>
</tr>
</tbody>
</table>