Adiabatic Array Logic

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***Abstract*— This paper presents an adiabatic logic, which is classified as rank-2 quasi-adiabatic. The proposed circuit which drives a sinusoidal power supply is based on array logic. The proposed logic consists of AND plane using transmission gate and wired-OR plane. Through the computer simulation, we show that the energy consumption of the proposed circuit is lower than that of CMOS logic circuit and lower than that of our previously proposed adiabatic logic circuit.**

I. Introduction

In the design of low-power VLSI circuits, adiabatic (or energy recovery) logic shows great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{dd}^2/2$. Numerous designs of adiabatic logic have been presented [1]–[11]. The different adiabatic logics that have been developed until now can be classified as Asymptotically adiabatic logics [1], [2], and Quasi-adiabatic logics [3]–[11]. The first category comprises structures that require computations to be reversible. The main idea behind the efficient operation of these architectures is to use the reverse computation for discharging in a controlled manner the capacitors that were charged during the forward computation. As their speed of operation approaches zero, these circuits dissipate asymptotically zero energy. Unfortunately, the high number of control signals they require results in relatively complex implementations. The second category is further classified into two groups: Rank-1 quasi-adiabatic [3], [5], [8], [10], [11] and Rank-2 quasi-adiabatic [4], [6], [7], [9]. The rank-1 adiabatic circuits use diodes to circumvent the requirement for reversible computations. The use of diodes results in relatively simple logic architectures with a small number of control lines. Diodes dissipate energy proportional to their threshold voltage, however, thus placing a lower bound on the efficiency of these circuits. The rank-2 is comprised of circuits in which state 0 or 1 is identical to released state and a certain amount of input information is destroyed during the instruction cycle. The energy dissipated per instruction cycle is proportional to CV_t^2, where V_t is the absolute value of the transistor threshold voltage. Nevertheless, energy dissipation can be reduced appreciably by lowering the rate of change of the driving voltage.

In this paper, we propose an adiabatic array logic, which is classified as rank-2 quasi-adiabatic. The proposed circuit which drives a sinusoidal power supply is based on array logic. The proposed logic consists of AND plane using transmission gate and wired OR plane. Then, through the computer simulation we show that the energy consumption of the proposed circuit is lower than that of CMOS logic circuit and lower than that of adiabatic logic circuit.

II. Adiabatic Logic

A. Conventional vis-a-vis Adiabatic Switching

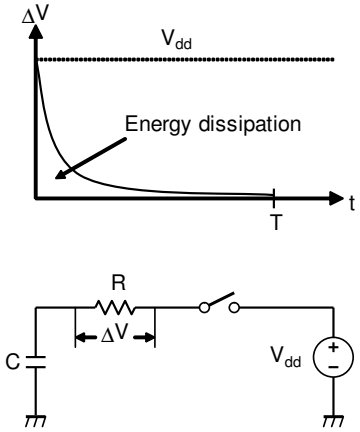
The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1(a). When a conventional CMOS inverter is set into a logical "1" state, a charge $Q = CV_{dd}$ is delivered to the load and the energy which the supply applies is $E_{applied} = QV_{dd} = CV_{dd}{}^2$, where V_{dd} is a DC power supply voltage. The energy stored into the load C is a half of the supplied energy:

$$E_{stored} = \frac{1}{2}CV_{dd}{}^2. \tag{1}$$

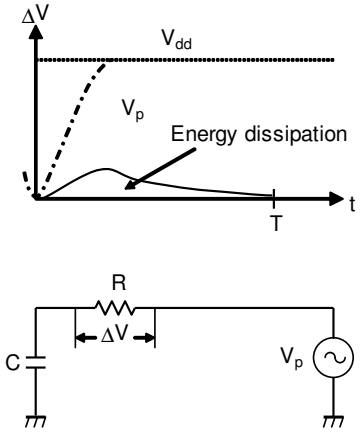
The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $QV_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge and discharge cycle:

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= \frac{1}{2}CV_{dd}{}^2 + \frac{1}{2}CV_{dd}{}^2 \\ &= CV_{dd}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency f_c $(= 1/T_c)$, where T_c is the period of the signal, then the power of the



(a) CMOS Charging.



(b) Adiabatic Charging.

Fig. 1. RC tree model.

CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T_c} = C{V_{dd}}^2 f. \tag{3}$$

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. The main idea in the adiabatic switching shown in Fig. 1(b) is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the $Q = CV_{dd}$ charge during the time period $\triangle T$, the energy dissipation in the channel resistance R is given by

$$\begin{aligned} E_{diss} &= \xi P \triangle T \\ &= \xi I^2 R \triangle T \\ &= \xi \left(\frac{CV_{dd}}{\triangle T} \right)^2 R \triangle T, \end{aligned} \tag{4}$$

where I is considered as the average of the current flowing to C, and ξ is a shape factor which depends on the shape of the clock edges [12]. It takes on the minimum value $\xi_{min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period $\triangle T$ is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [1].

B. Adiabatic Array Logic

Figure 2 shows the proposed adiabatic array logic. This circuit which drives a sinusoidal power supply is based on array logic, and also consists of AND plane using transmission gate and wired OR plane. For a given input, the proposed adiabatic gate is operating as parallel transmission gate chains, which for each time slot have at least one path between the sinusoidal power clock, and the output node set to a logic one. To analyze the circuit, a transmission gate in the ON state is represented with a linear model made up of a resistance R and one capacitance at the output node C [as shown in Fig. 1(b)]. In [12], an ON resistance R has been proposed as follows:

$$\begin{aligned} R = \frac{1}{V_{dd}} \Bigg[& \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}} \ln \left(\frac{V_{dd} - V_{tn}}{V_{dd} - V_{tn} - |V_{tp}|} \right) \\ & + \frac{1}{\mu_p C_{ox} \frac{W_p}{L_p}} \ln \left(\frac{V_{dd} - |V_{tp}|}{V_{dd} - V_{tn} - |V_{tp}|} \right) \\ & + \frac{1}{\mu_p C_{ox} \frac{W_p}{L_p} - \mu_n C_{ox} \frac{W_n}{L_n}} \ln \left(\frac{\mu_p \frac{W_p}{L_p}}{\mu_n \frac{W_n}{L_n}} \right) \Bigg]. \end{aligned} \tag{5}$$

Capacitance C is evaluated assuming the triode region for both transistors and is given by

$$C = W \left(\frac{1}{2} L + \Delta L \right) C_{ox} + C_{jB} \tag{6}$$

where, ΔL is the overlap and capacitance C_{jB} is due to the junction between the diffusion and the bulk. Therefore, the power dissipation of proposed circuit depends on the equivalent series ON resistance.

A potential weakness of proposed circuit is high output impedance in AND plane because output impedance and series ON resistance are equivalent. Hence, the number of cascade stage is "*four*" or less from the standpoint of achieving higher output voltage.

III. Simulation Results

To verify the practical applicability of the proposed adiabatic array circuit, we design and simulate an 1-bit full adder.

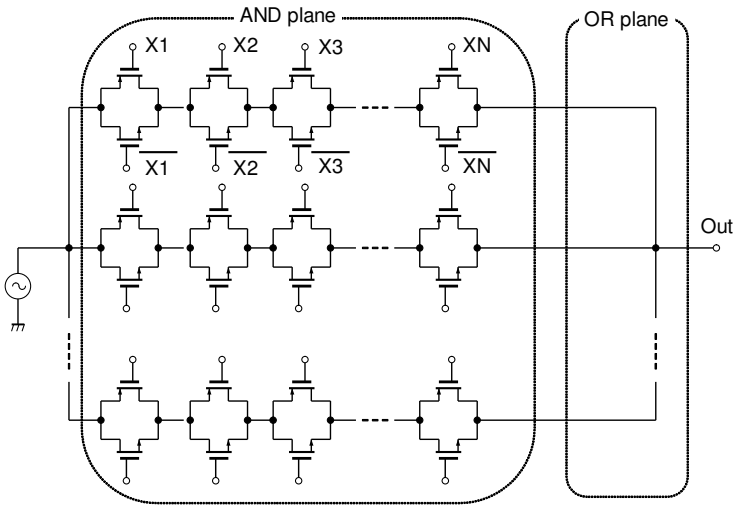


Fig. 2. Proposed adiabatic array circuit.

Operations of a full adder are defined by the Boolean equations for the sum and carry signals:

$$S_i = X_i Y_i C_i + \overline{X_i} Y_i \overline{C_i} + X_i \overline{Y_i}\ \overline{C_i} + \overline{X_i}\ \overline{Y_i} C_i, \quad (7)$$

$$C_{i+1} = XY + XC_i + YC_i, \quad (8)$$

where X_i, Y_i, and C_i are the inputs to the i-th full adder stage, and S_i and C_{i+1} are the sum and carry outputs from the i-the stage, respectively. From the above equation we could actually design the 1-bit full adder which is composed of adiabatic array logic as shown in Fig. 3.

The 1-bit full adder of adiabatic logic as shown in Fig. 3 was tested by SPICE simulation using an 0.18 μm, 1.8 V CMOS standard process technology. The transistor size W/L is 0.6 μm/0.18 μm for both of the PMOS and NMOS transistors. Simulations were carried out for the following purposes: the proposed 1-bit full adder array logic power consumptions in comparison with the circuit obtained using CMOS static, CMOS array, IPAL [9], and 2PADCL [10]. To evaluate the power savings in the circuits, we compute the energy consumption E, which is defined as follows:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} V_{p_i} I_{p_i} \right) dt, \quad (9)$$

where T_s $(=1/f_s)$ is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current, and i is a number of power supply. Therefore, E is equal to the net energy flowing into the circuit from the power supply line.

The SPICE simulation results obtained for the proposed 1-bit full adder are shown in Fig. 4. Figure 4(a) shows the driving voltage of the sinusoidal supply clock, Figs. 4(b) and (c) demonstrate the input signals which is a CMOS compatible rectangular pulse, and Fig. 4(d) shows the output waveform.

Table I summarizes power dissipation and the number of transistors of each logics. From this table some of the results can be summarized as follows:

1) The power dissipation of the proposed circuit is the best of the five logic circuits.
2) The proposed circuit offers approximately the same number of transistors as IPAL.

IV. Conclusion

In this paper we have presented adiabatic logic using array logic circuit. The proposed adiabatic array logic has constructed by AND plane using transmission gate and Wired-OR plane. From the simulation results, we have found that the power dissipation of proposed adiabatic logic is lower than that of other logic style, and also the number of logic gate is the same as IPAL.

The authors will further evaluate noise performance (i.e. voltage scaling, fun-in/fun-out, etc) in the proposed array logic, as for our future work.

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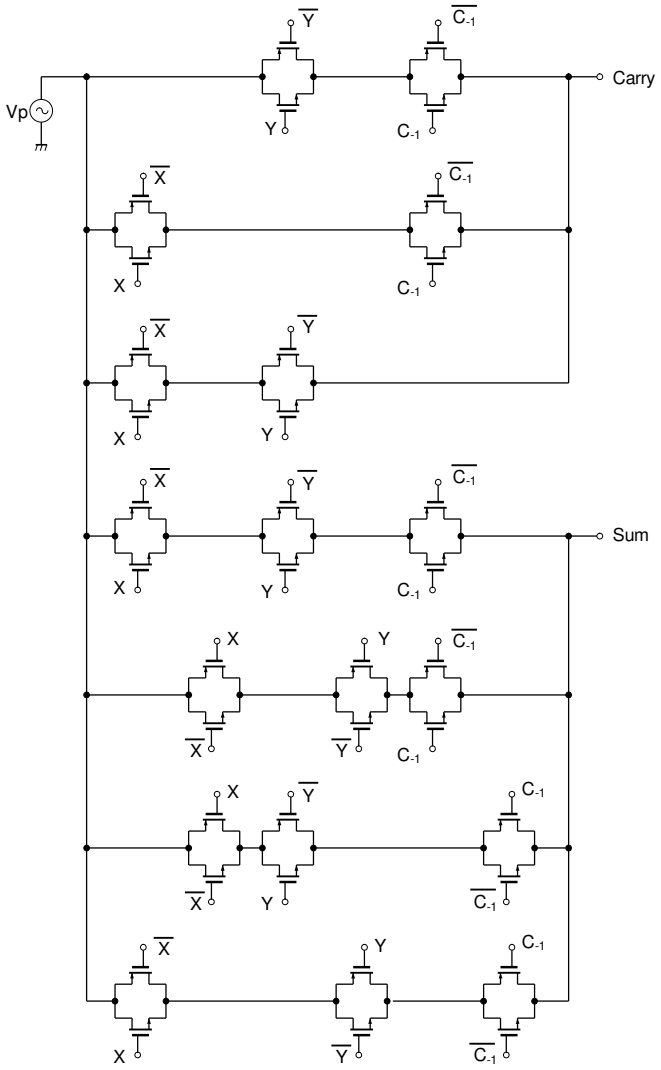

Fig. 3. The proposed adiabatic array 1-bit full adder.

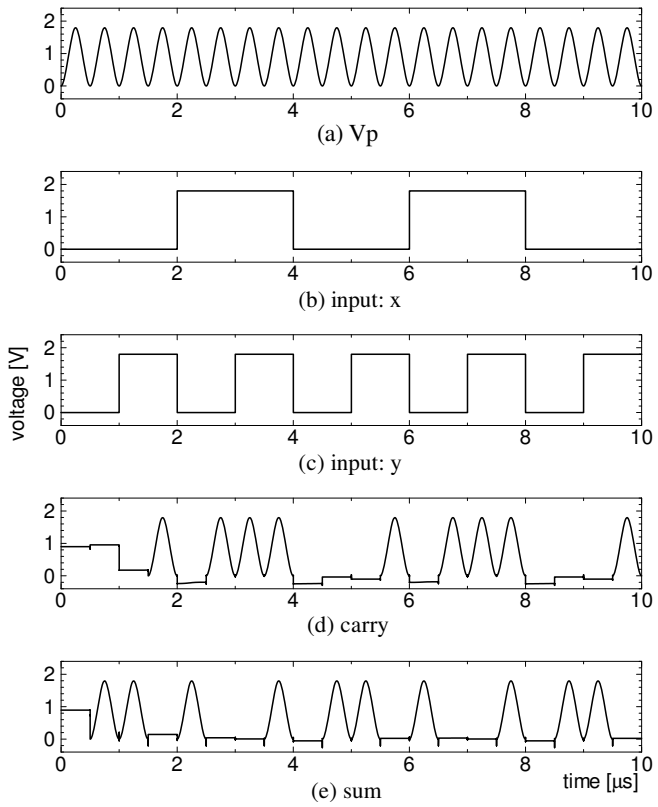

Fig. 4. Input/output waveforms and supply waveform of the proposed 1-bit full adder.

TABLE I
COMPARISON OF POWER DISSIPATION AND NUMBER OF TRANSISTORS IN 1-BIT FULL ADDER

	Power dissipation	Number of transistors
CMOS static	282 fJ	56
CMOS array	1.1 nJ	62
IPAL [9]	142 fJ	34
2PADCL [10]	140 fJ	80
Adiabatic array	1.4 fJ	36

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