A 70MHz Multiplierless FIR Hilbert Transformer in 0.35μm CMOS Standard-cell Technology

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Introduction

The digital Hilbert transformer is a basic signal processing operator used in numerous application domains, for example, telecommunications, wireless multimedia communication, speech/audio/image processing, and many more. The digital Hilbert transformers can be realized of either the infinite impulse response (IIR) and the finite impulse response (FIR) filters. Since the Hilbert transformer is required to strictly shift the phase of signal by 90 degrees over wide range frequency, we will have the choice of using FIR with linear. However, the Hilbert transformer using FIR filter is attributable to its amplitude ripple and large circuit scale.

The primary source of complexity in FIR digital filters is the filter coefficients. These coefficients have been traditionally represented in binary number format and implemented as constant multipliers. One way of implementing more efficient multipliers is to represent the filter coefficients in canonic signed digit (CSD) format. Thus, in the case of using FIR digital filter, we can save the circuit scale of Hilbert transformer.

Aim

We present high performance implementations for digital Hilbert transformers based on our recently proposed constant multiplier using vertical and horizontal common sub-expression elimination (CSE) techniques.

Results

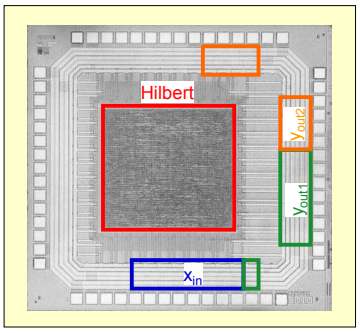

Figure 2 *VLSI chip diephoto.*

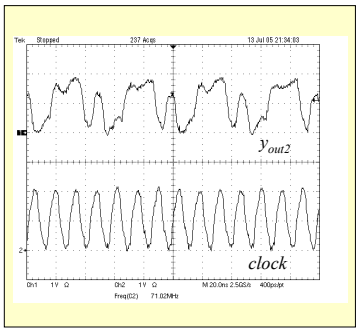

Figure 3 *MSB output at 71MHz.*

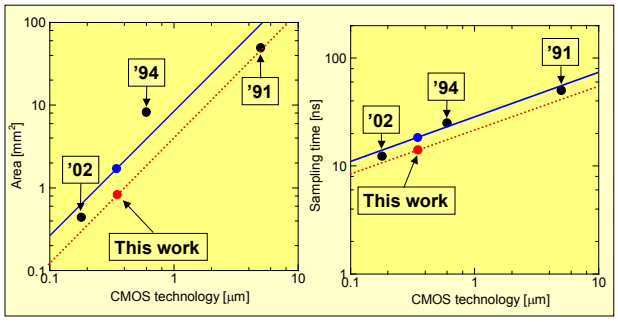

Figure 4 *Comparison of previous reference works.*

Table 1 *Chip specifications.*

Technology	0.35μm 3-metal, 2-poly
Supply	3.3V
Core size	0.86mm²
Transistors	32988
Clock Frequency	71MHz
Filter order	31-taps
Power dissipation	263mW @ 70MHz

Method

To achieve the above mentioned objectives, we design the FIR Hilbert transformer according to the following three steps.

- As the digital FIR filter features a flexibility, a testability, low-cost and high performance, the Hilbert transformer consists of a digital FIR filter.
- Using different number representation such as CSD code, the FIR filter can be increased the speed.
- Using optimization transformations on signal flow graph technique such as common sub-expression elimination, we can reduce the VLSI area required for the FIR Hilbert transformer.

Under above conditions, we obtain the final FIR Hilbert transformer structure shown in Fig.1, which requires a smaller chip size, a faster speed, and has less power dissipation after ASIC implementation.

The multiple constant multiplication (MCM) problem determines how sub-expression elimination can be applied to the set of constant multipliers so that the number of shifts and additions required for implementations is minimized. CSE as a way to tackle the MCM problems is as a possible method for the optimization of finite duration FIR filter area through the reduction of the multiplier block logic. In general, the goal of CSE can be defined as follows.

- Identify multiple patterns in the coefficient set.
- Remove these patterns and calculate them only once.

Our CSE techniques have been proposed an efficient way to find the correct bit-patterns for horizontal and vertical CSEs. In the proposed technique, the problem of reducing the costs is stated as the problem of minimizing the weighted sum of the numbers of the registers and adders/subtractors which are needed to perform all of the multiplications. That is, the objective cost function (*CF*) to be minimized is written as:

$$CF = \beta \times N_{reg} + \gamma \times N_{as}, \qquad (1)$$

where N_{reg} and N_{as} are the number of registers and adders/subtracters, respectively, β and γ are weights.

Using the proposed method, we can reduce the MCM area of the FIR filter by an average 20%.

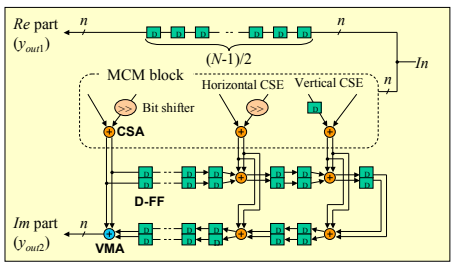

Figure 1 *Block-diagram of Hilbert transformer.*

Conclusions

We have presented the design and implementation of a 31-tap FIR Hilbert transform digital filter chip. The architecture has been based on a computation sharing multiplier using vertical and horizontal common sub-expression elimination techniques. The chip has been implemented by using a 0.35μm CMOS process technology with the area of 0.86mm². The chip has been a clock frequency of 71MHz and a power consumption of 263mW at 70MHz.

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Acknowledgment

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