4×4-Bit Array Multiplier using Two Phase Clocked Adiabatic Static CMOS Logic

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Abstract— This paper proposes a low-power 4×4-bit array multiplier design employing two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. From the simulation results, at transition frequencies of 5 to 50 MHz, 4×4-bit 2PASCL multiplier shows a maximum of 64% reduction in power dissipation to that with a static CMOS. The simulation is performed using SPICE implemented with 1.2 μm standard CMOS technology.

I. INTRODUCTION

In recent times, one of the major goals in VLSI design is a long battery operating life. In conventional CMOS circuits, power dissipation primarily occurs during device switching. Sudden flow of current through channel resistive elements resulting in one-half the supplied energy, i.e., $(\frac{1}{2})C_L V_{dd}^2$ dissipated at each transition. The approach of a low-power circuit system by implementing the concept of adiabatic switching and energy recovery has been applied where an early adiabatic logic family has been proposed [1].

At the earlier stage of the 2PASCL [2], we have designed and simulated 2PASCL fundamental logic family. In this paper, we simulate the 4×4-bit array 2PASCL multiplier and compare the dissipated power to the CMOS multiplier. This design will soon be fabricated implemented using 1.2 μm standard process. The W/L of the transistors are 5.0μm/1.2μm.

II. RESULTS

Figure 1 demonstrates the power dissipation comparison of 4×4-bit array 2PASCL multiplier with CMOS at 5 to 50 MHz transition frequencies. The simulation result shows that up to 64% reduction in the power dissipation is achieved when using 2PASCL topology. From our observations, for more than 50 MHz transition frequency, 2PASCL is not showing a good output signal. Relatively higher dissipation than CMOS when operated at less than 5 MHz. Thus, 5 to 50 MHz is considered the optimum range for 4×4-bit array 2PASCL multiplier. In Fig. 2, we present the layout design of 2PASCL 1-bit half adder and 1-bit full adder, respectively.

III. CONCLUSION

In this paper we designed and simulated a 4×4-bit two-phase clocked adiabatic CMOS logic (2PASCL) multiplier circuit. The simulation results show that power consumption in the 2PASCL multiplier is considerably less than that in
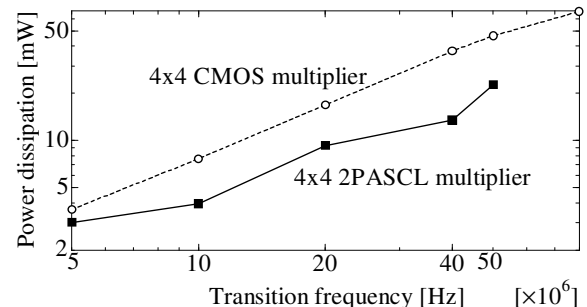

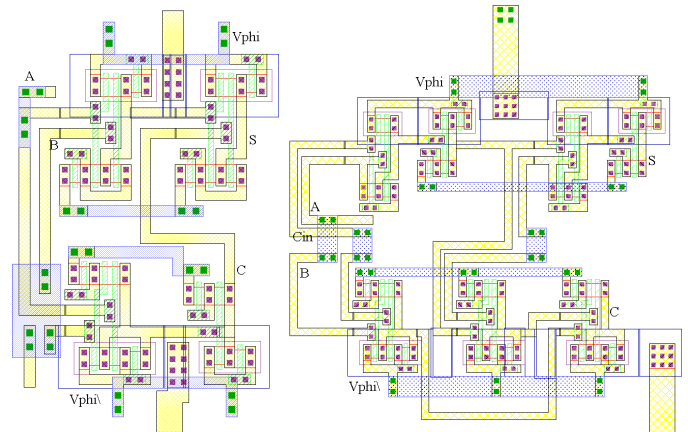Fig. 1. Power dissipation comparison of the 4×4-bit array multiplier of 2PASCL and CMOS.

Fig. 2. (left) Layout design of 2PASCL 1-bit half adder and (left) 2PASCL 1-bit full adder.

a CMOS. When the input frequency is simulated from 5 to 50 MHz, the 2PASCL multiplier logic dissipates minimally as only one-third of the power dissipated by a static CMOS logic circuit. The measurement results of the actual device power consumption will be discussed in the next publication.

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