Theoretical Analysis of Power Clock Generator based on the Switched Capacitor Regulator for Adiabatic CMOS Logic

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***Abstract*—This paper reports an analytical method of a power clock generator based on a switched capacitor circuit which is used in adiabatic logic. We derive first an equivalent circuit model of the switched capacitor circuit. We then discuss the design optimization of the capacitance ratio. Finally, we show that the analytical results agree rather well with the SPICE simulation results.**

I. Introduction

In the design of low-power VLSI circuits, adiabatic (or energy recovery) logic shows great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{dd}{}^2/2$, where C is a load capacitance, and V_{dd} is a supply voltage of VLSI circuit. Numerous designs of adiabatic logic have been presented [1]–[10]. The driving of adiabatic logic requires adiabatic controlled sources of voltage. The adiabatic drivers fall into two classes: resonant driver and staircase driver. The resonant driver generates the pulses from the natural oscillations of a resonator, with power recovery provided by a dc-voltage source. The generators of quasi-sinusoidal pulses can be built around the simplest resonator, namely, an LC circuit. Such a driver has been used in Refs. [2]–[7], and [9]. On the other hand, a staircase driver was first proposed by L. J. Svensson and J. G. Koller [1], and then has been used in Refs. [8] and [10]. The staircase driver includes a switched capacitor regenerator, which has a tank capacitor for restoring the charge energy. In Ref. [8], the properties and stability of a switched capacitor regenerator has been discussed, however, has not been discussed yet from the viewpoint of design optimization.

This paper reports an analytical method of the switched capacitor regenerator. We derive first an equivalent circuit model of the switched capacitor circuit, and then propose analytical methods for step voltage difference. Finally, we show that the analytical results agree rather well with the SPICE simulation results.

II. Conventional CMOS Logic vs. Adiabatic Logic

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load capacitance C. The pull-up and pull-down networks are actually MOS transistors in series with the same load C. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1. When a conventional CMOS inverter is set into a logical "1" state, a charge $Q = CV_{dd}$ is delivered to the load and the energy which the supply applies is $E_{applied} = QV_{dd} = CV_{dd}{}^2$. The energy stored into the load C is a half of the supplied energy:

$$E_{stored} = \frac{1}{2}CV_{dd}{}^2. \tag{1}$$

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= \frac{1}{2}CV_{dd}{}^2 + \frac{1}{2}CV_{dd}{}^2 \\ &= CV_{dd}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency $f\ (= 1/T)$, where T is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T} = CV_{dd}{}^2 f. \tag{3}$$

The main idea in an adiabatic switching shown in Fig. 2 is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver or oscillator. If a constant current source delivers the $Q = CV_{dd}$ charge during the time period $\triangle T$, the energy dissipation in

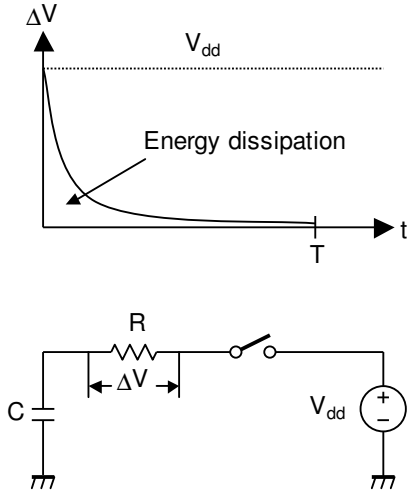

Fig. 1. Charging an RC tree with a switch.

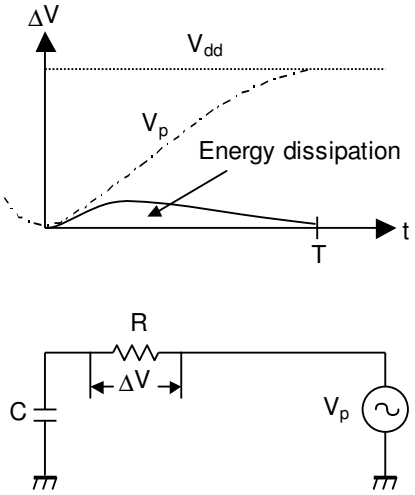

Fig. 2. Adiabatic charging of an RC tree.

the channel resistance R is given by

$$\begin{aligned} E_{diss} &= \xi P \triangle T \\ &= \xi I^2 R \triangle T \\ &= \xi \left(\frac{C V_{dd}}{\triangle T} \right)^2 R \triangle T, \end{aligned} \tag{4}$$

where ξ is a shape factor which depends on the shape of the clock edges [11]. It takes on the minimum value $\xi_{min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period $\triangle T$ is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [1].

III. Switched Capacitor Regenerator

A. Concept

The switched capacitor regenerator (SCR) was first proposed by L. Svensson and J. G. Koller [1]. This regenerator uses a source voltage and $N-1$ capacitors, so that an N-step waveform is created and the charging energy is reduced to $1/N$. Figure 3 shows the switched capacitor regenerator used in the analysis ($N = 4$). The regenerator consists of a voltage source, five pass transistors that have input signals from Clk0 to Clk4, three tank capacitors C_1, C_2, and C_3, and load capacitor C_L. Figure 4 depicts its operation. Transistors are turned on as Clk0, Clk1, Clk2, Clk3, Clk4, Clk3, Clk2, Clk1, Clk0. This is done repeatedly and the output voltage V_{out} becomes a step waveform.

With i running from 1 to N, a load capacitor is switched from one voltage source to the nest. It is clearly seen from the V–Q diagram as shown in Fig. 5 that energy dissipated per cycle is

$$W = qV_{dd} = \frac{C{V_{dd}}^2}{N}. \tag{5}$$

Since the voltage source are free from dissipation, except for the N-th source, they can be represented by capacitors with high capacitances (such as C_1 in Fig. 3). This circuit has a self-stabilizing property: the voltages across the capacitors C_1 are set to required levels automatically. In Ref. [8], Nakata has proved that each step of the output voltage of the regenerator circuit with $(N-1)$ capacitors always settles to the voltage of

$$\frac{i}{N} \cdot V \ (i = 0, 1, 2, \cdots, N) \tag{6}$$

regardless of the initial condition, in the case of $C_n \gg C_L$ where C_n is the tank capacitor. However, the tank capacitor C_n cannot be immoderately increased as capacitor size is affected by the chip die.

In the next subsection, we will explain an equivalent circuit model of the SCR, and then discuss the design optimization of the capacitance ratio.

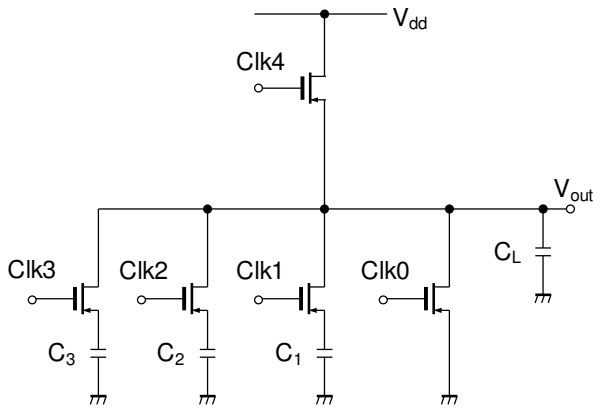

Fig. 3. Switched Capacitor Re-generator (SCR).

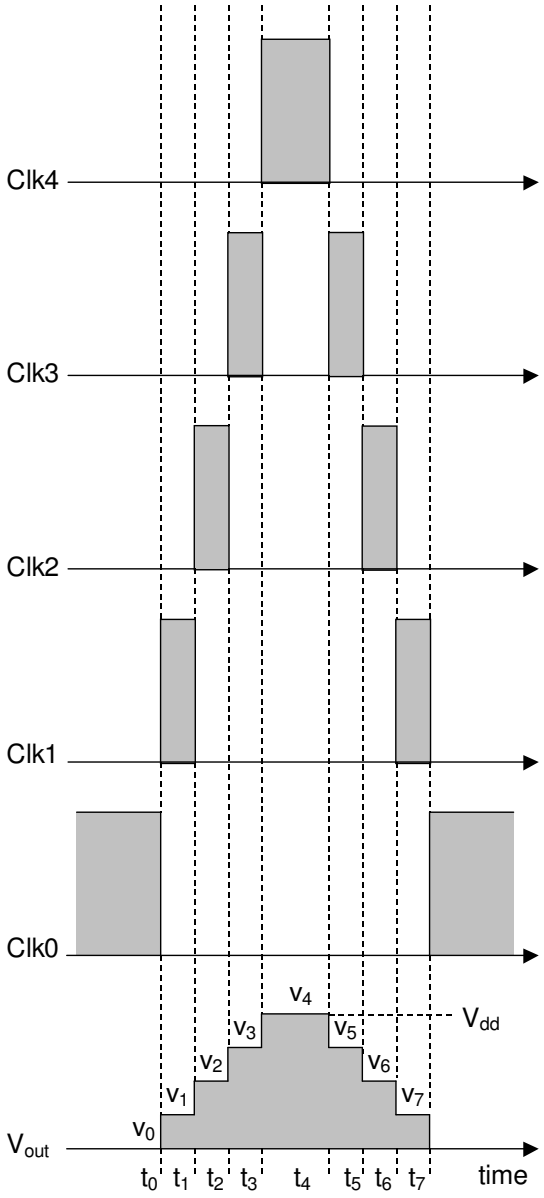

Fig. 4. Output waveform of SCR.

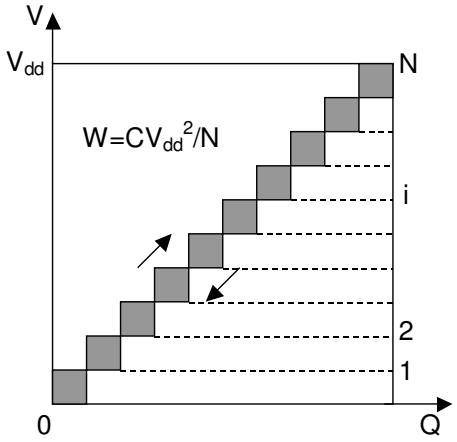

Fig. 5. V–Q diagram of SCR.

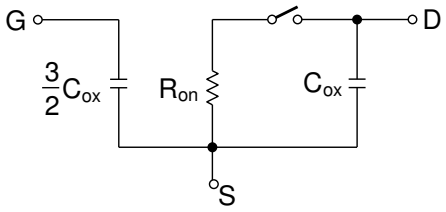

Fig. 6. NMOS equivalent digital model.

B. Theoretical Analysis

The switching behavior of the NMOS transistor can be generalized by examining the parastic capacitances and resistances, and so we consider the NMOS switch shown in Fig. 6 with the equivalent digital model [12]. Note that the effective input and output capacitances of the NMOS are $C_{in} = \frac{3}{2}C_{ox}$ and $C_{out} = C_{ox}$, respectively. We then can draw the equivalent circuit of Fig. 7, by using the equivalent digital model of the NMOS.

At first, we consider the voltage on a capacitance C_1. An electric charge in C_1 can be determined from the equivalent circuit as follows:

$$\begin{aligned} Q_{t01} &= C_1 V_7 + \frac{3}{2}C_{ox}(V_7 - V_{\rm clk1}) \\ &\quad + C_{ox}(0 - V_{C_1 0}) + C_{ox}(0 - V_{C_2 0}) \\ &\quad + C_{ox}(0 - V_{C_3 0}) + C_{ox}(0 - V_{dd}), \end{aligned} \tag{7}$$

where $V_{C_x y}$ $(y = 1, 2, \cdots, n)$ is voltage of the node capacitance C_x $(x = 1, 2, \cdots, n)$, and then total capacitance Q_{t1} has

$$\begin{aligned} Q_{t1} &= V_1 \left(C_L + \frac{5}{2}C_{ox} \right) + C_1 V_1 \\ &\quad + \frac{3}{2}C_{ox}(V_1 - V_{\rm clk1}) + C_{ox}(V_1 - V_{C_2 1}) \\ &\quad + C_{ox}(V_1 - V_{C_3 1}) + C_{ox}(V_1 - V_{dd}). \end{aligned} \tag{8}$$

Equations (7) and (8) follow from charge conservation,

$$\begin{aligned} V_1 &= \frac{V_7 \left(\frac{3}{2}C_{ox} + C_1 \right)}{C_L + 7C_{ox} + C_1} \\ &\quad + \frac{C_{ox}(V_{C_2 1} + V_{C_3 1} - V_{C_1 0} - V_{C_2 0} - V_{C_3 0})}{C_L + 7C_{ox} + C_1}. \end{aligned} \tag{9}$$

C_{ox} is much smaller than C_L (or C_n) and so the second term in the above equation can be neglected as compared to the

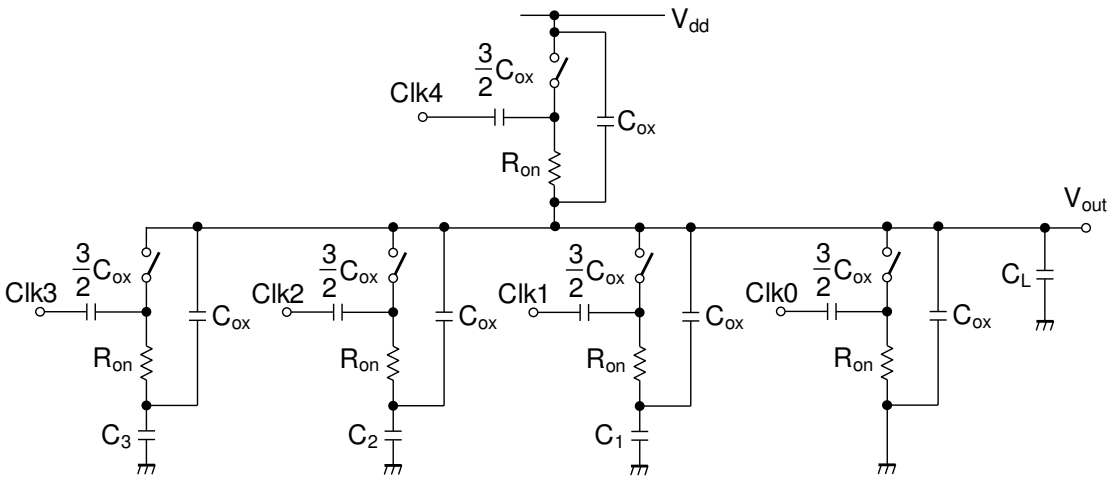

Fig. 7. SCR equivalent circuit.

first term. Finally, we have the following equation.

$$V_1 = \frac{\frac{3}{2}C_{ox}V_7 + C_1V_7}{C_L + 7C_{ox} + C_1} \simeq \frac{C_1V_7}{C_L + 7C_{ox} + C_1}. \quad (10)$$

From the above equation, we can see that a terminal voltage V_1 is not equal to V_7. Of course, it is possible to get the same voltage if C_1 is much larger than C_L, however, the tank capacitor C_1 cannot be immoderately increased as capacitor size is affected by the chip die.

The other voltage conditions are also as follows:

$$V_0 = 0, \quad (11)$$

$$V_2 = \frac{V_1(C_L + C_{ox}) + C_2V_6}{C_L + 7C_{ox} + C_2}, \quad (12)$$

$$V_3 = \frac{V_2(C_L + C_{ox}) + C_3V_5}{C_L + 7C_{ox} + C_3}, \quad (13)$$

$$V_4 = V_{dd}, \quad (14)$$

$$V_5 = \frac{V_{dd}(C_L + C_{ox}) + C_3V_3}{C_L + 7C_{ox} + C_3}, \quad (15)$$

$$V_6 = \frac{V_5(C_L + C_{ox}) + C_2V_2}{C_L + 7C_{ox} + C_2}, \quad (16)$$

$$V_7 = \frac{V_6(C_L + C_{ox}) + C_1V_1}{C_L + 7C_{ox} + C_1}. \quad (17)$$

From equations (12) and (16), (13) and (15), we can also see that the terminal voltages V_2 and V_6 (or V_3 and V_5) are not equal.

C. Comparison of Analysis and Simulation Results

In order to compare the analysis with simulation results, the SCR was simulated in a 1.2 μm CMOS n-well technology provided by On-Semi conductor. The transistor size W/L is 5.0 μm/1.2 μm for both of the PMOS and the NMOS transistors. C_{ox} is calculated from SPICE parameters. The tank and load capacitances are be implemented as poly-poly capacitance.

Figure 8 shows the comparison of analysis with simulation results. We show that the analytical results agree rather well with the SPICE simulation results. From the viewpoint of CMOS implementation, however, we think that Fig. 8(a) has an optimized condition because of poly-poly capacitance.

IV. Conclusion

We have reported an analytical method of a power clock generator based on a switched capacitor circuit which is used in adiabatic logic. We have derived first an equivalent circuit model of the switched capacitor circuit. Then, we have discussed the design optimization of the capacitance ratio. Finally, we show that the analytical results agree rather well with the SPICE simulation results. From the viewpoint of 1.2μm CMOS implementation, the capacitance ratio $C_L : C_n$ has been set at $0.1 : 1.0$.

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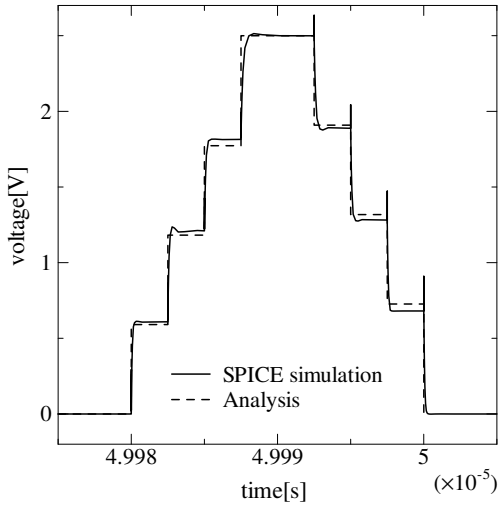
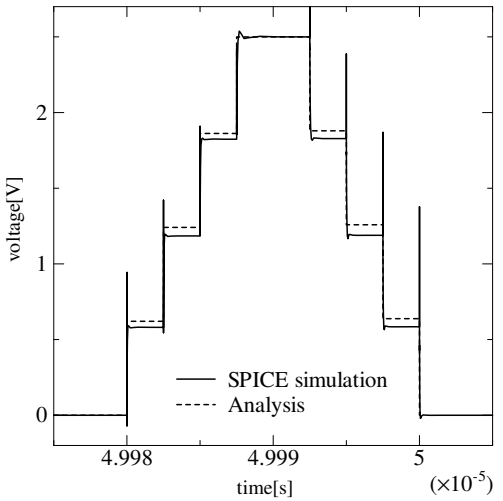
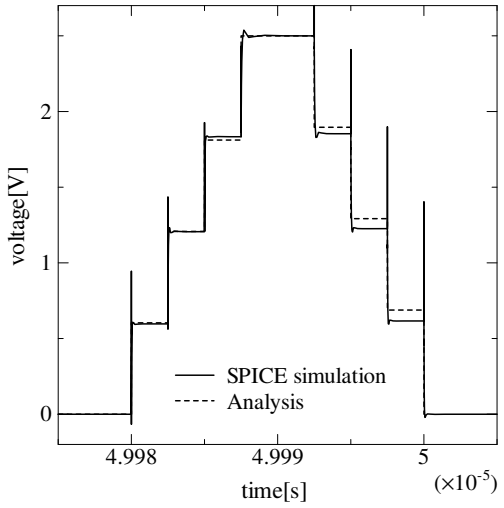


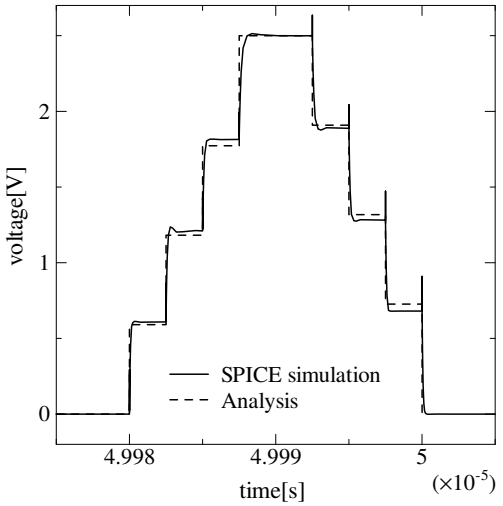
(a) $C_L = 0.1$ pF, $C_n = 1$ pF.



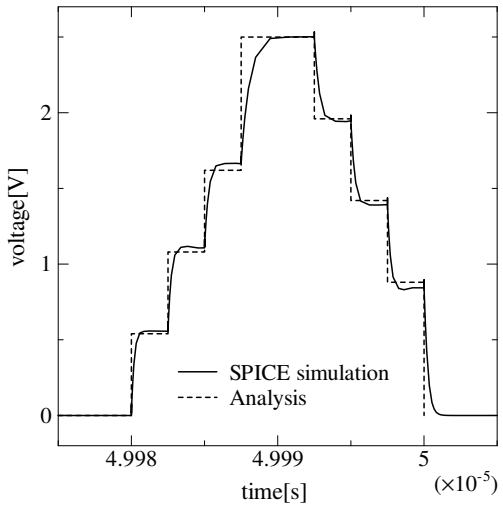
(b) $C_L = 0.01$ pF, $C_n = 5$ pF.



(c) $C_L = 0.01$ pF, $C_n = 1$ pF.



(d) $C_L = 0.1$ pF, $C_n = 5$ pF.



(e) $C_L = 0.5$ pF, $\mathrm{C_n} = 1$ pF.

Fig. 8. Comparison of analysis with simulation results.

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