# Two-phase Clocked CMOS Adiabatic Logic

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**Abstract**

This paper presents a new adiabatic logic which drives two-phase clocking. The proposed adiabatic logic (2PC2AL) uses two trapezoidal-wave pulses and resembles behavior of static CMOS. The structure of 2PC2AL can be directly derived from static CMOS logic circuits. We also propose a trapezoidal-wave generator compatible to 2PC2AL. The proposed clock generator is based on the switched capacitor circuit. From the simulation results, we show that the energy consumption of the proposed circuit is lower than that of CMOS logic circuits in the range of from 1 to 100 MHz, and the 4-bit multipliers also are about 30–50% lower.

**Keywords**

adiabatic logic, trapezoidal-wave, low power, multiplier.

## 1 INTRODUCTION

In the design of low-power VLSI circuits, adiabatic (or energy recovery) logic shows great potential, because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $CV_{dd}{}^2/2$. Numerous designs of adiabatic logic have been presented [1]–[10]. The different adiabatic logics that have been developed until now can be classified as *Asymptotically adiabatic* logics [1], [2], and *Quasi-adiabatic* logics [3]–[10]. The first category comprises structures that require computations to be reversible. The main idea behind the efficient operation of

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these architectures is to use the reverse computation for discharging in a controlled manner the capacitors that were charged during the forward computation. As their speed of operation approaches zero, these circuits dissipate asymptotically zero energy. Unfortunately, the high number of control signals they require results in relatively complex implementations. The second category is further classified into two groups: *Rank-1 quasi-adiabatic* [3], [7]–[10] and *Rank-2 quasi-adiabatic* [4]–[6]. The rank-1 adiabatic circuits uses diodes to circumvent the requirement for reversible computations. The use of diodes results in relatively simple logic architectures with a small number of control lines. Diodes dissipate energy proportional to their threshold voltage, however, thus placing a lower bound on the efficiency of these circuits. The rank-2 is comprised of circuits in which state $0$ or $1$ is identical to released state and a certain amount of input information is destroyed during the instruction cycle. The energy dissipated per instruction cycle is proportional to $CV_t^2$, where $V_t$ is the absolute value of the transistor threshold voltage. Nevertheless, energy dissipation can be reduced appreciably by lowering the rate of change of the driving voltage.

In this paper, we propose a clocked CMOS adiabatic logic, which is classified as rank-2 quasi-adiabatic. The proposed circuit which drives two trapezoidal-wave pulses is called 2-Phase Clocked CMOS Adiabatic Logic (2PC2AL). The 2PC2AL circuits can be directly converted from static CMOS circuits without drastically increasing the circuit area. We also propose a new scheme of generating supply clocks based on the switched capacitor circuit. Then, through the computer simulation we show that the energy consumption of the 2PC2AL circuit is lower than that of CMOS logic circuit.

## 2 Adiabatic Logic

### 2.1 Conventional vs. Adiabatic Switching

The conventional switching can be understood by using a simple CMOS inverter. The CMOS inverter can be considered to consist of a pull-up and pull-down networks connected to a load (or internal) capacitance $C$. The pull-up and pull-down networks are actually MOS transistors in series with the same load $C$. Both transistors can be modeled by an ideal switch in series with a resistor which is equal to the corresponding channel resistance of the transistor in the saturation mode, as shown in Fig. 1(a). When a conventional CMOS inverter is set into a logical "1" state, a charge $Q = CV_{dd}$ is delivered to the load and the energy which the supply applies is $E_{applied} = QV_{dd} = CV_{dd}{}^2$. The energy stored into the load $C$ is a half of the supplied energy:

$$E_{stored} = \frac{1}{2} CV_{dd}{}^2. \tag{1}$$

The same amount of energy is dissipated during the discharge process in the NMOS pull-down network because no energy can enter the ground rail $Q \times V_{gnd} = Q \times 0 = 0$. From the energy conservation law, a conventional CMOS logic emits heat and, in this way, it wastes energy in every charge-discharge cycle:

$$\begin{aligned} E_{total} &= E_{charge} + E_{discharge} \\ &= \frac{1}{2}CV_{dd}{}^2 + \frac{1}{2}CV_{dd}{}^2 \\ &= CV_{dd}{}^2. \end{aligned} \tag{2}$$

If the logic is driven by a certain frequency $f$ $(= 1/T)$, where $T$ is the period of the signal, then the power of the CMOS gate is determined as:

$$P_{total} = \frac{E_{total}}{T} = CV_{dd}{}^2 f. \tag{3}$$

The main idea in an adiabatic switching shown in Fig. 1(b) is that transitions are considered to be sufficiently slow so that heat is not emitted significantly. This is made possible by replacing the DC power supply by a resonance LC driver, an oscillator, a clock generator, etc. If a constant current source delivers the $Q = CV_{dd}$ charge during the time period $\triangle T$, the energy dissipation in the channel resistance $R$ is given by

$$\begin{aligned} E_{diss} &= \xi P \triangle T \\ &= \xi I^2 R \triangle T \\ &= \xi \left( \frac{CV_{dd}}{\triangle T} \right)^2 R \triangle T, \end{aligned} \tag{4}$$

where $\xi$ is a shape factor which depends on the shape of the clock edges [11]. It takes on the minimum value $\xi_{min} = 1$ if the charge of the load capacitor is DC modulated. For a sinusoidal current, $\xi = \pi^2/8 = 1.23$. The above equation indicates that when the charging period $\triangle T$ is indefinitely long, in theory, the energy dissipation is reduced to zero. This is called an adiabatic switching [1].

### 2.2 Proposed Adiabatic Logic

The proposed 2PC2AL inverter is shown in Fig. 2(a), where the inverter is operated with complementary phases of power supply signals. The supply waveform consists of three modes as shown in Fig. 2(b):

1) output *evaluation*: power supplies are activated by slow ramp signals, computing the input information;
2) *hold*: the value of the output signal is read by the next stage;

3) output *recovery*: the clocks are deactivated, returning the output to its previous value.

Figure 3 shows three computational cycles of the 2PC2AL inverter. When input signal $V_{in}$ is from low (0) to high (1), the NMOS turns on and therefore $V_{out}$ flows $\overline{V_p}$ in the evaluation phase. In this phase, the output node voltage is the following condition:

$$\begin{aligned} V_{out} &= V_p \quad (V_{dd}/2 < V_{out} \leq V_{dd}) \rightarrow \\ & \quad \overline{V_p} \quad (0 \leq V_{out} < V_{dd}/2). \end{aligned} \tag{5}$$

When $V_{in}$ is from high to low, the PMOS turns on and therefore $V_{out}$ flows $V_p$ in the recovery phase. In this phase, the output node voltage is th following condition:

$$\begin{aligned} V_{out} &= \overline{V_p} \quad (0 \leq V_{out} < V_{dd}/2) \rightarrow \\ & \quad V_p \quad (V_{dd}/2 < V_{out} \leq V_{dd}). \end{aligned} \tag{6}$$

For the other condition $0 \rightarrow 0$ (or $1 \rightarrow 1$), the output node voltage swings $\overline{V_p}$ (or $V_p$). Just as the inverter is compatible with adiabatic mode under the condition shown in Fig. 3, other gates (e.g. 2input-NAND, NOR) and complex gates operate with adiabatic mode under the same condition.

In this circuit, since Drain-Source voltage $V_{ds}$ may be different from $0$ in the evaluation phase, switching is not fully adiabatic. Moreover, the output voltage does not return to the desired precharge value in the recovery phase. Therefore, the energy waste in non-adiabatic transport of charge (or discharge) is

$$E_{\mathrm{non-adi}} = \frac{1}{2} C \Delta^2, \tag{7}$$

where $\Delta$ is the value of $V_{tn}$ or $|V_{tp}|$. The energy dissipation of proposed logic finally is as following:

$$\begin{aligned} E_{\mathrm{total}} &= E_{\mathrm{diss}} + E_{\mathrm{non-adi}} \\ &= \xi \frac{(CV_{dd})^2 R}{\triangle T} + \frac{1}{2} C \Delta^2. \end{aligned} \tag{8}$$

### 2.3 Power Clock Generator

The proposed circuit has required two trapezoidal-wave, $V_p$ and $\overline{V_p}$. In this paper, we propose an approximately trapezoidal-wave generator using a Switched Capacitor Regenerator (SCR) [12]. The proposed generator consists of pulse generator and SCR, as shown in Fig. 4. The pulse generator is operated that transistors of SCR (Fig. 5(a) and

(b)) are turned on as Clk0, Clk1, Clk2, Clk3, Clk4, Clk3, Clk2, Clk1, Clk0. This is done repeatedly and the output voltage $V_p$ (or $\overline{V_p}$) becomes a step waveform in Fig. 6. With $i$ running from 1 to $N$, a load capacitor is switched from one voltage source to the nest. It is clearly seen from the $V$–$Q$ diagram as shown in Fig. 7 that energy dissipated per cycle is

$$W = qV_{dd} = \frac{C{V_{dd}}^2}{N}. \tag{9}$$

Since the voltage source are free from dissipation, except for the $N$-th source, they can be represented by capacitors with high capacitances (such as $C_1$ in Fig. 5). This circuit has a self-stabilizing property: the voltages across the capacitors $C_1$ are set to required levels automatically. In Ref. [13], Nakata has proved that each step of the output voltage of the regenerator circuit with $(N-1)$ capacitors always settles to the voltage of

$$\frac{i}{N} \cdot V \ (i = 0, 1, 2, \cdots, N) \tag{10}$$

regardless of the initial condition, in the case of $C_n \gg C_L$ where $C_n$ is the tank capacitor. However, the tank capacitor $C_n$ cannot be immoderately increased as capacitor size is affected by the chip die.

### *2.3.1 Theoretical Analysis*

In Ref. [14], we have reported an analytical method of a SCR. The switching behavior of the NMOS transistor can be generalized by examining the parastic capacitances and resistances, and so we consider the NMOS switch shown in Fig. 8 with the equivalent digital model [15]. Note that the effective input and output capacitances of the NMOS are $C_{in} = \frac{3}{2}C_{ox}$ and $C_{out} = C_{ox}$, respectively. We then can draw the equivalent circuit of Fig. 9, by using the equivalent digital model of the NMOS. At first, we consider the voltage on a capacitance $C_1$. An electric charge in $C_1$ can be determined from the equivalent circuit as follows:

$$Q_{t01} = C_1 V_7 + \frac{3}{2}C_{ox}(V_7 - V_{\mathrm{clk1}}) + C_{ox}(0 - V_{C_1 0}) + C_{ox}(0 - V_{C_2 0}) + C_{ox}(0 - V_{C_3 0}) + C_{ox}(0 - V_{dd}), \tag{11}$$

where $V_{C_x y}$ $(y = 1, 2, \cdots, n)$ is voltage of the node capacitance $C_x$ $(x = 1, 2, \cdots, n)$, and then total capacitance $Q_{t1}$ has

$$Q_{t1} = V_1 \left( C_L + \frac{5}{2}C_{ox} \right) + C_1 V_1 + \frac{3}{2}C_{ox}(V_1 - V_{\mathrm{clk1}}) + C_{ox}(V_1 - V_{C_2 1}) + C_{ox}(V_1 - V_{C_3 1}) + C_{ox}(V_1 - V_{dd}). \tag{12}$$

Equations (11) and (12) follow from charge conservation,

$$V_1 = \frac{V_7\left(\frac{3}{2}C_{ox} + C_1\right)}{C_L + 7C_{ox} + C_1} + \frac{C_{ox}(V_{C_21} + V_{C_31} - V_{C_10} - V_{C_20} - V_{C_30})}{C_L + 7C_{ox} + C_1}. \tag{13}$$

$C_{ox}$ is much smaller than $C_L$ (or $C_n$) and so the second term in the above equation can be neglected as compared to the first term. Finally, we have the following equation.

$$V_1 = \frac{\frac{3}{2}C_{ox}V_7 + C_1V_7}{C_L + 7C_{ox} + C_1} \tag{14}$$

$$\simeq \frac{C_1V_7}{C_L + 7C_{ox} + C_1}. \tag{15}$$

From the above equation, we can see that a terminal voltage $V_1$ is not equal to $V_7$. Of course, it is possible to get the same voltage if $C_1$ is much larger than $C_L$, however, the tank capacitor $C_1$ cannot be immoderately increased as capacitor size is affected by the chip die.

The other voltage conditions are also as follows:

$$V_0 = 0, \tag{16}$$

$$V_2 = \frac{V_1(C_L + C_{ox}) + C_2V_6}{C_L + 7C_{ox} + C_2}, \tag{17}$$

$$V_3 = \frac{V_2(C_L + C_{ox}) + C_3V_5}{C_L + 7C_{ox} + C_3}, \tag{18}$$

$$V_4 = V_{dd}, \tag{19}$$

$$V_5 = \frac{V_{dd}(C_L + C_{ox}) + C_3V_3}{C_L + 7C_{ox} + C_3}, \tag{20}$$

$$V_6 = \frac{V_5(C_L + C_{ox}) + C_2V_2}{C_L + 7C_{ox} + C_2}, \tag{21}$$

$$V_7 = \frac{V_6(C_L + C_{ox}) + C_1V_1}{C_L + 7C_{ox} + C_1}. \tag{22}$$

From equations (17) and (21), (18) and (20), we can also see that the terminal voltages $V_2$ and $V_6$ (or $V_3$ and $V_5$) are not equal.

#### *2.3.2 Comparison of Analysis and Simulation Results*

In order to compare the analysis with simulation results, the SCR was simulated in a $1.2\ \mu\mathrm{m}$ CMOS n-well technology provided by On-Semi conductor. The transistor size $W/L$ is 5.0 $\mu$m/1.2 $\mu$m for both of the PMOS and the NMOS transistors. $C_{ox}$ is calculated from SPICE parameters. The tank and load capacitances are be implemented as poly-poly capacitance.

Figure 10 shows the comparison of analysis with simulation results. We show that the analytical results agree rather well with the SPICE simulation results. From the viewpoint of CMOS implementation, however, we think that Fig. 10(a) has an optimized condition because of poly-poly capacitance.

## 3 Simulation Results of Proposed Adiabatic Logic

### 3.1 Four Inverter Chain

The chain of four inverters was tested by SPICE simulation using a 0.35 $\mu$m CMOS process technology provided by TSMC. The transistor size $W/L$ is $1.50/0.35$ for both of the PMOS and NMOS transistors. To evaluate the power savings in the circuits, we compute the energy consumption $E$, which is defined as follows:

$$E = \int_0^{T_s} \left( \sum_{i=1}^{n} (V_{p_i} \times I_{p_i}) \right) dt, \tag{23}$$

where $T_s (= 1/f_s)$ is the period of the primary input signal, $V_p$ is the power supply voltage, $I_p$ is the power supply current, and $i$ is a number of power supply. Therefore, $E$ is equal to the net energy flowing into the circuit from the power supply line. As discussed in Ref. [10], energy transfers between the controlling signals and the controlled signals. Within a cycle (charging and discharging), energy flows into the circuit and is recovered back from it. The level difference of $E$ in two (or more) consecutive cycles reflects the energy loss in a full cycle. The effect of energy transfers between the controlling and the controlled signals leads to the energy transferring from one phase of power supply to another. Therefore, we have to compute the "Net energy" by summing up the energy in power supply lines.

Figure 11 shows the comparison of energy consumption. This result shows that the proposed 2PC2AL reduces the energy consumption by about two times as compared to CMOS logic in the 1 MHz to 100 MHz range. However, the proposed adiabatic logic is not adiabatic mode over 100 MHz and so the power consumption of the proposed circuit is much higher than that of the CMOS circuit.

### 3.2 4-bit Multiplier

In order to validate the functionality of the 2PC2AL logic, the 4×4-bit multipliers were simulated in a $1.2$ $\mu$m CMOS n-well technology provided by On-Semi conductor. The transistor size $W/L$ is 5.0 $\mu$m/1.2 $\mu$m for both of the PMOS and the NMOS transistors. In order to confirm the speed versus power consumption, Booth array [16], Baugh-Wooley [17], and Wallace tree [18] type multipliers were used.

Simulation results for the 2PC2AL multiplier are compared to a static CMOS multiplier using same logic implementation and same transistor size. Simulations were performed using randomly generated input vectors which are independent of each other. The probability of being "1" (and "0") for each input in each clock cycle is also 0.5, and the probability that an input switches in the following cycle is also 0.5.

Table 1 summarizes the power consumption for three different multipliers. In SPICE simulation and for operating frequencies ranging from 1 MHz to 120 MHz, our adiabatic multipliers are dissipated about 30–50% less energy than their static CMOS counterparts.

## 4 Conclusion

In this paper, we have presented a two-phase clocked CMOS adiabatic logic. The proposed adiabatic logic has used two trapezoidal-wave pulses, which is classified as rank-2 quasi-adiabatic. The performance of 2PC2AL has short switching delay and relatively high throughput. Our simulation result with 2PC2AL circuits has indicated a factor of about two reductions in energy consumption under 100 MHz range.

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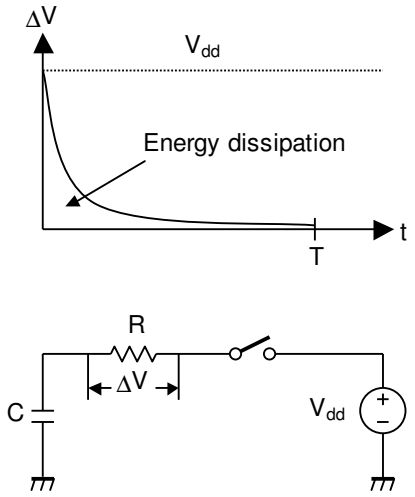
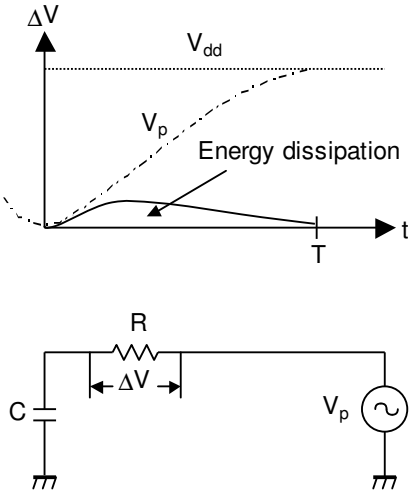
Table 1
Comparison of different 4-bit multipliers between CMOS and Adiabatic.

| | Booth array | Baugh-Wooley | Wallace tree |
|---|---|---|---|
| CMOS | 5.6 mW @ 100 MHz (100%) | 5.3 mW @ 50 MHz (100%) | 6.6 mW @ 120 MHz (100%) |
| Adiabatic | 3.5 mW @ 100 MHz (62.5%) | 2.8 mW @ 50 MHz (52.8%) | 4.5 mW @ 120 MHz (68.2%) |

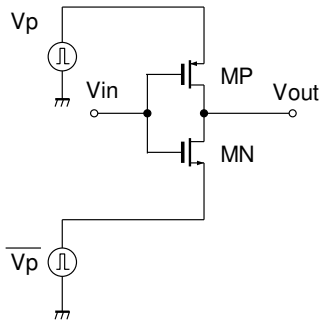



(a) CMOS Charging.

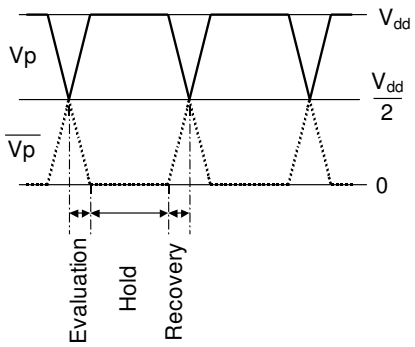



(b) Adiabatic Charging.

Fig. 1. $RC$ tree model.

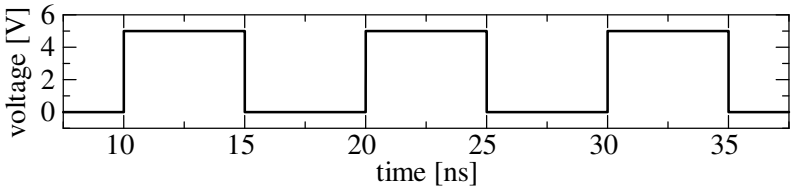



(a) Inverter logic.

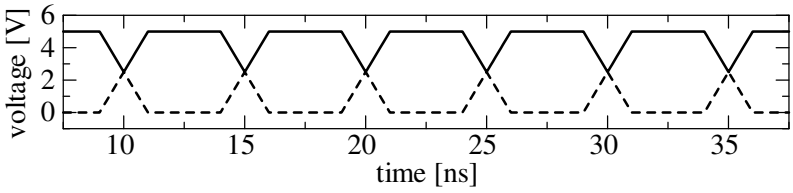



(b) Clocking waveform.

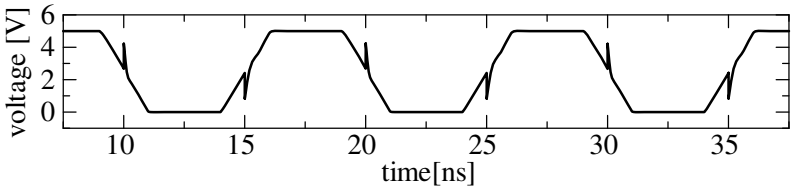
Fig. 2. 2-phase clocked CMOS adiabatic logic (2PC2AL).




(a) Input $V_{in}$.




(b) Clock $V_p$, $\overline{V_p}$.




(c) Output $V_{out}$.

Fig. 3. Output waveform of 2PC2AL.

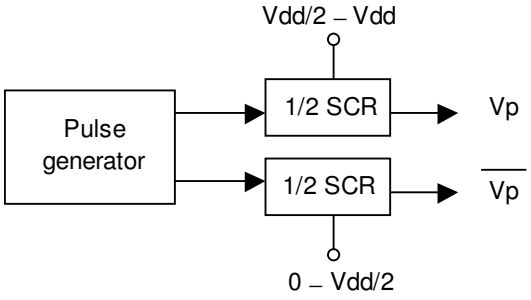
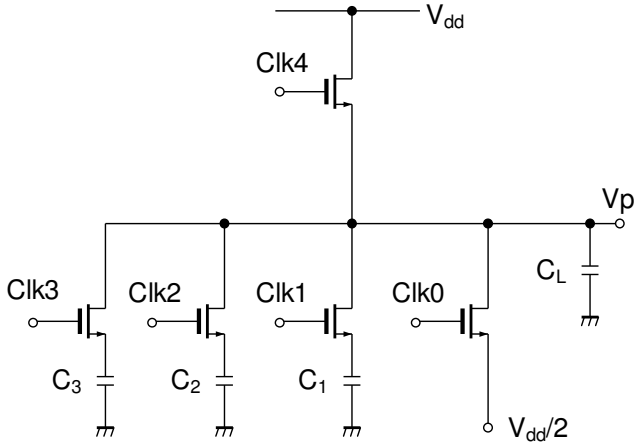
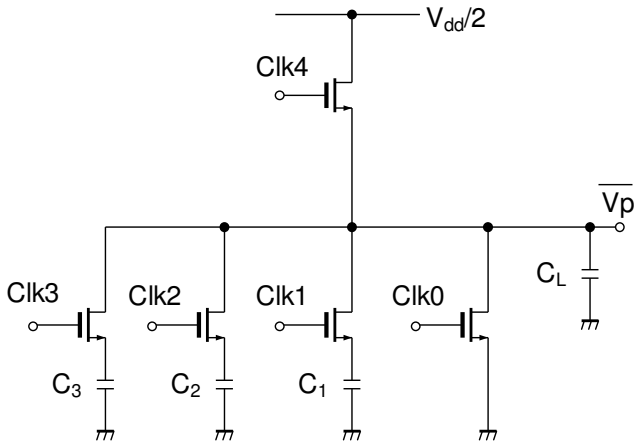



Fig. 4. Block diagram of trapezoidal-wave generator.




(a) $V_p$ generator circuit.




(b) $\overline{V_p}$ generator circuit.

Fig. 5. Trapezoidal-wave generator circuit.

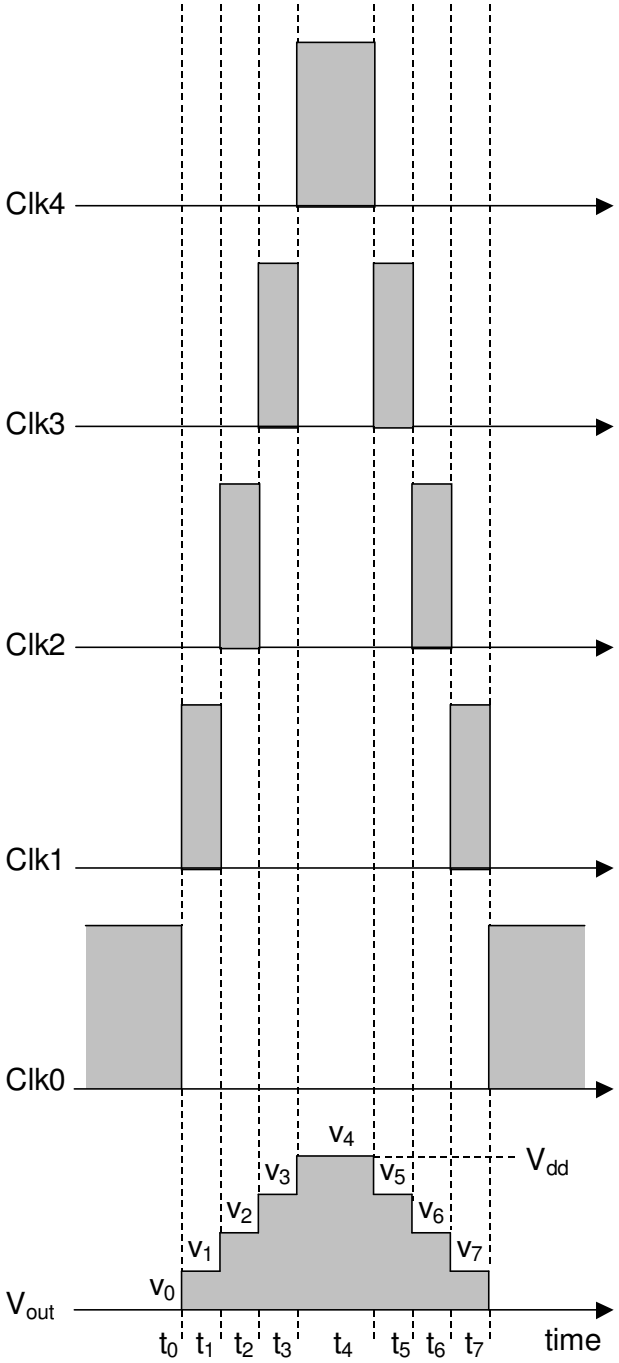



Fig. 6. Output waveform of SCR.

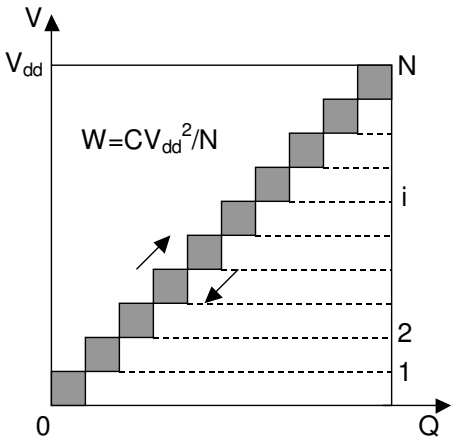



Fig. 7. $V$–$Q$ diagram of SCR.

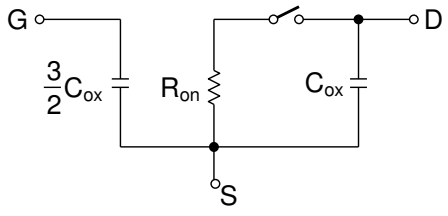



Fig. 8. NMOS equivalent digital model.

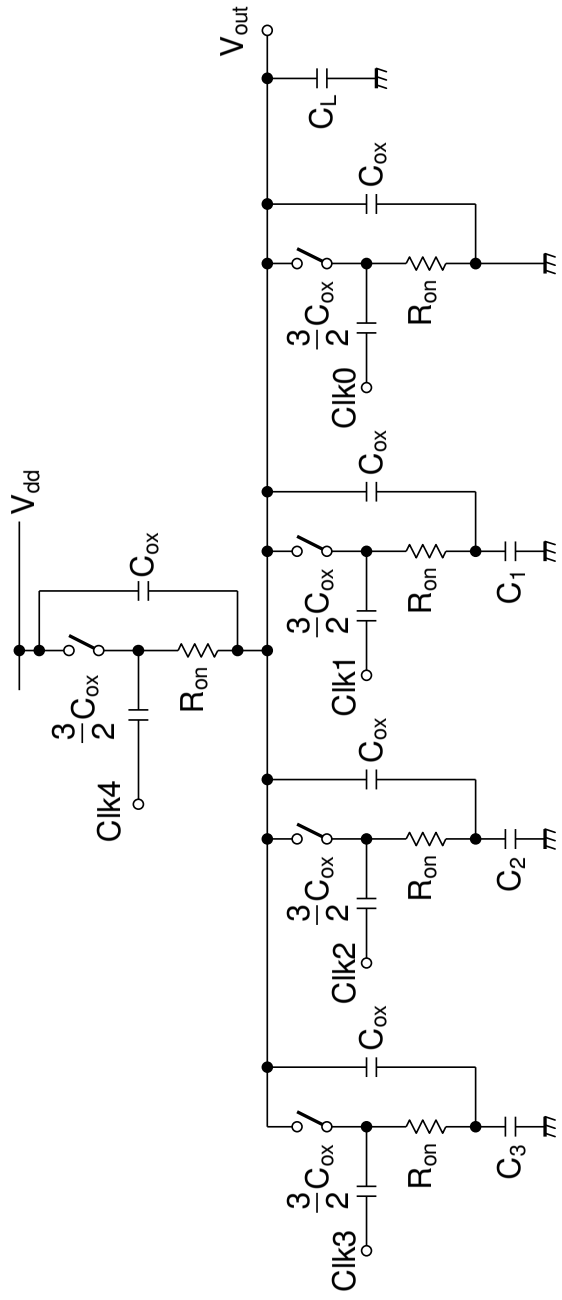
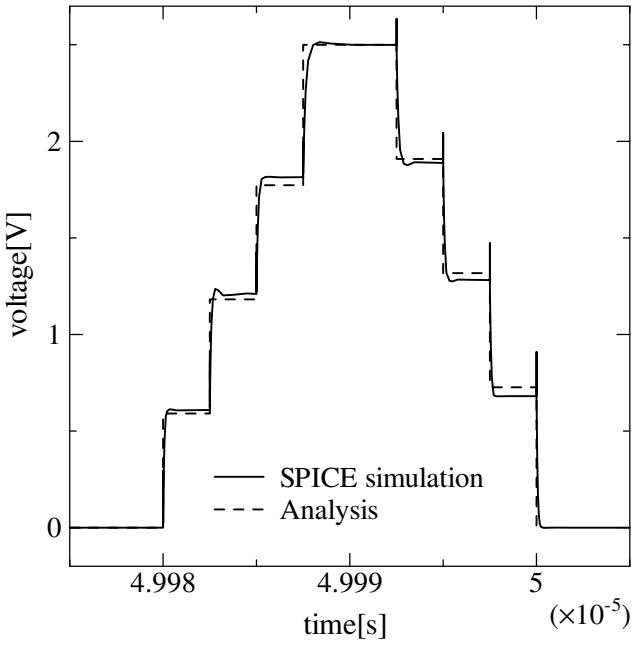
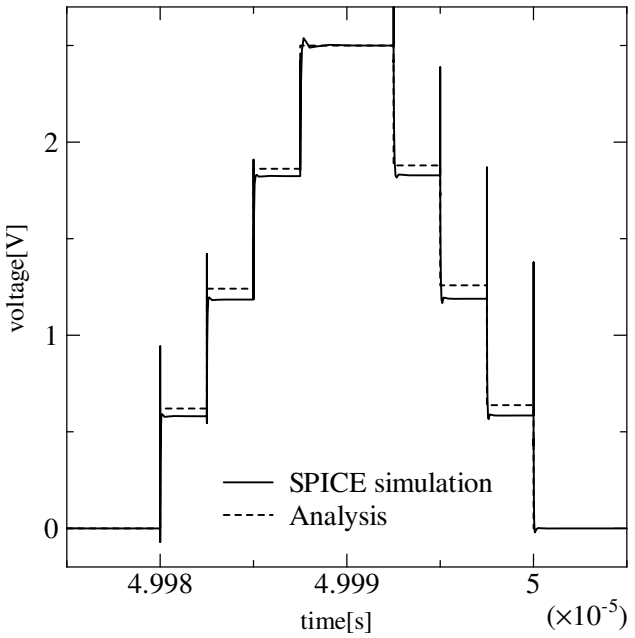


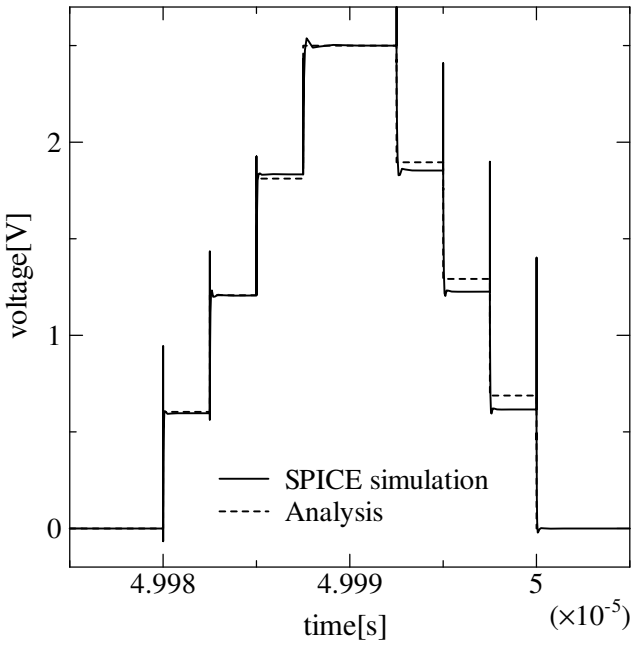

Fig. 9. SCR equivalent circuit.



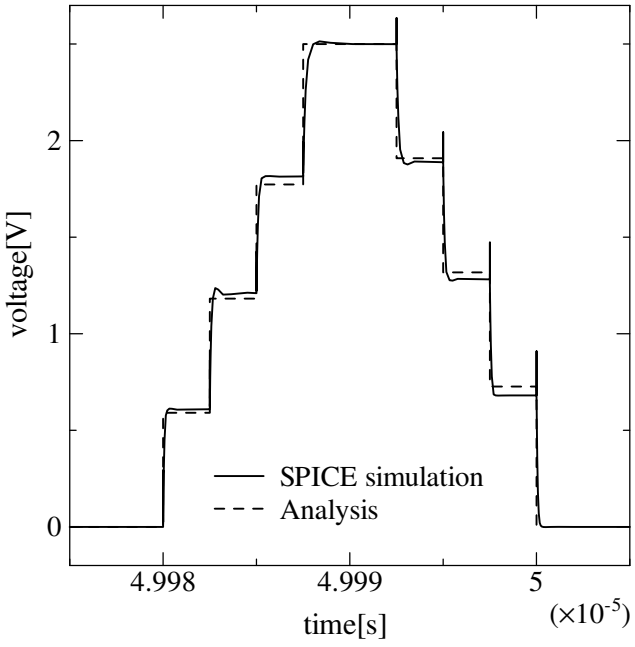

(a) $C_L = 0.1$ pF, $C_n = 1$ pF.



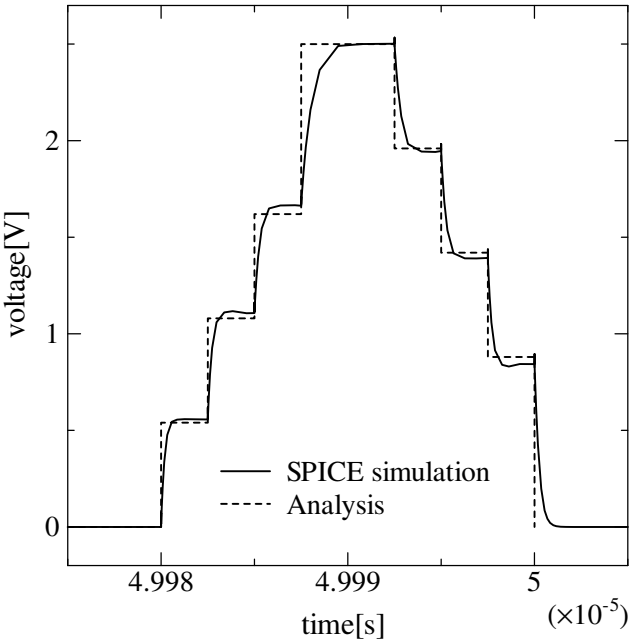

(b) $C_L = 0.01$ pF, $C_n = 5$ pF.




(c) $C_L = 0.01$ pF, $C_n = 1$ pF.




(d) $C_L = 0.1$ pF, $C_n = 5$ pF.




(e) $C_L = 0.5$ pF, $\mathrm{C_n} = 1$ pF.

Fig. 10. Comparison of analysis with simulation results.

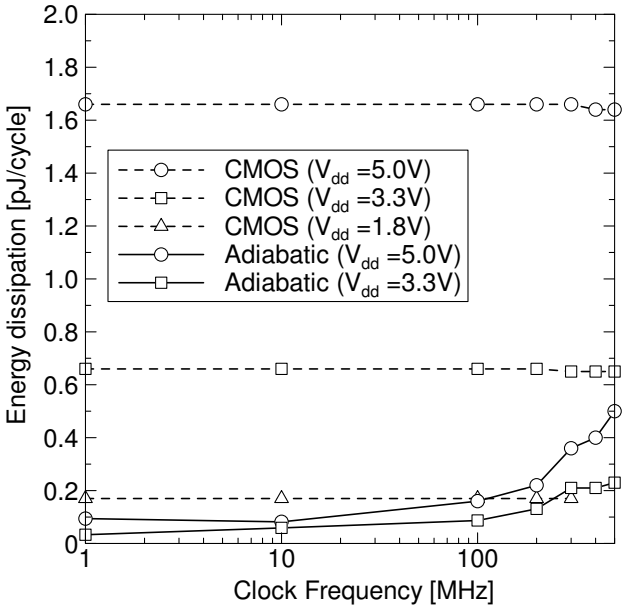



Fig. 11. Comparison of power dissipation of the four inverter chains.