CMOS Analog Matched Filter for DS-CDMA System Based on Operational Amplifier

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Abstract: This paper describes a novel matched filter for CDMA system. The structure of the proposed matched filter mainly consists of two parts: a voltage follower with a sample hold circuit and a selector which changes the pseudo-noise sequence (PN sequence) pattern. From the results of SPICE simulation, it is found that the proposed matched filter operates at the chiprate of 5 MHz and over. In addition, we found that the power consumption of the proposed matched filter is 47.3 mW at 5 V power supply. The proposed matched filter has been realized in a 1.2 μm CMOS process.

1. Introduction

Direct Spread Code Division Multiple Access (DS-CDMA) system is widely used for data communication systems, wireless communication systems and cellular communication systems, etc [1]. In the DS-CDMA system, the matched filter is required for a receiver to cross-correlate the received signal with a locally generated PN sequence. Recent papers have been reported: digital type [2], charge coupled device (CCD) type [3], surface acoustic wave (SAW) type [4] and analog type [5]. For CCD and SAW types, the insertion loss of the CCD/SAW filter is a serious problem. Also, in order to set the fixed comparative code at the receiving end, we need another comparative pattern when a spread code is changed [1].

In this paper, we describe a novel matched filter for CDMA system. Since the proposed filter consists of the voltage follower realized by using an operational amplifier (OP-amp), the output signal is little attenuated. In addition, the proposed filter can change comparative pattern by using the selector.

2. Proposed Circuit

2.1 Matched filter

The matched filter for a DS-CDMA calculates the correlation between a received signal and a PN code. The matched filter output is as following:

$$C[i] = F_r[i] \otimes F_s[i] = \sum_{k=-\infty}^{\infty} F_r[i]F_s[i+k] \qquad (1)$$

where $F_r[i]$ and $F_s[i]$ are the received and the spread sequences, respectively. Let n_s denotes the length of corresponding sequence $F_s[i]$, the length of $C[i]$ could be as long as

$$n_s = 2^n - 1 \ (\forall n \in \mathbb{N}). \qquad (2)$$

Figure 1 shows the block diagram of the proposed matched filter. First, the spread signal is shifted and extracted by the delay circuit. Secondly, the same extracted data from each delay circuit corresponds to the spread pattern through the selector. Finally, the correlation value is calculated by the OP-amp.

2.2 Sample Hold Circuit

The proposed sample hold circuit which consists of the delay element is shown in Fig. 2 and transistor size of the sample hold circuit is summarized in Table 1. In Fig. 2, the proposed circuit consists of the voltage follower realized by using the OP-amp. Also, because this circuit have high input resistance and low output resistance, it does not affect the behavior of other circuits. As a result, the sampled signal without attenuation is transmitted to the next stage in the delay circuit.

The principle of sample hold are the following:

Principle (a) : Sample statement
When the CMOS Switch (SW) is ON, the load capacitor C is charged by the input signal V_{in}.

Principle (b) : Hold statement
When the SW is OFF, the value of the load capacitor keeps the last data.

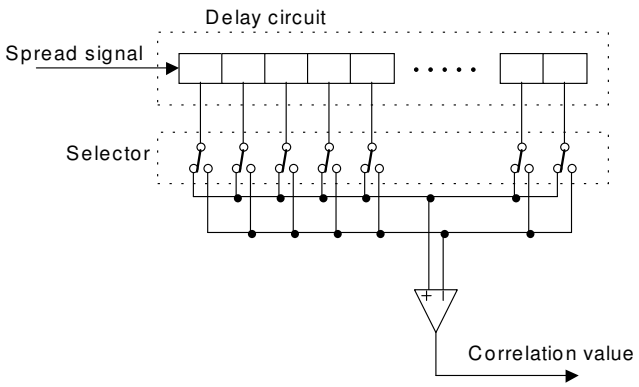

Figure 1. Block diagram of the proposed matched filter.

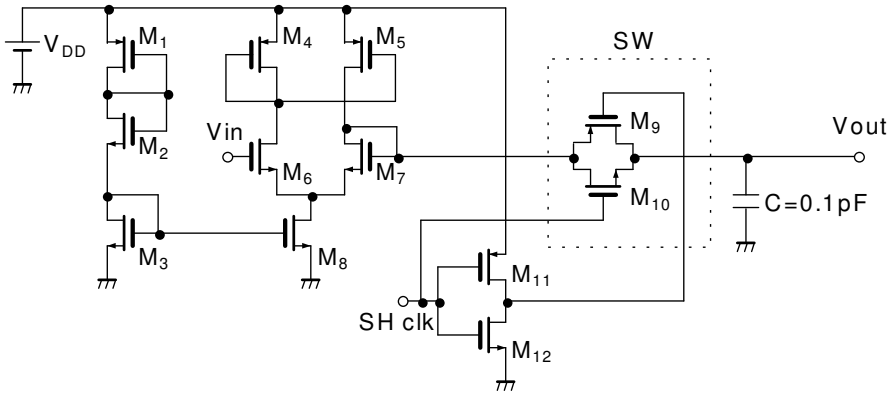

Figure 2. Sample hold circuit.

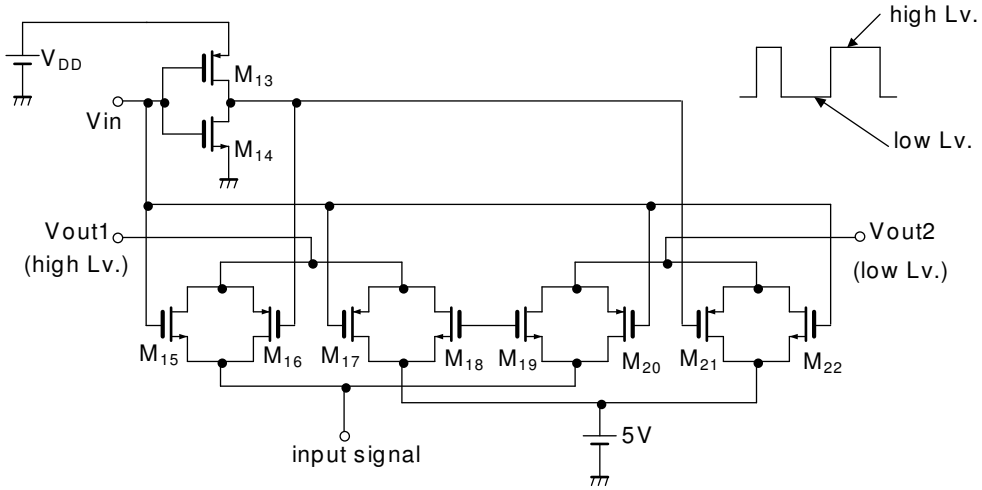

Figure 3. Selector circuit.

Table 1. Transistor size of the sample hold circuit.

Name	L/W [μm]
M_1	$5.0/40$
M_2	$5.0/10$
$M_3 - M_8$	$5.0/20$
M_9, M_{10}	$1.5/2.0$

Table 2. Transistor size of the selector circuit.

Name	L/W [μm]
M_{13}	$1.5/20$
M_{14}	$1.5/10$
$M_{15} - M_{22}$	$1.5/2.0$

2.3 Partten Selector Circuit

Figure 3 shows a selector circuit (which changes with the pattern). Table 2 summarizes the transistor size of the selector circuit. The proposed selector has two output ports. It is necessary to identify two types (i.e. high and low level) of the input signals. Thus, we have any PN sequence patterns by using such a circuit.

To control the select circuit, first, the PN sequence (which sets at sending end of transmission) input to port the V_{in}. Secondly, the input signal is divided into two levels. Finally, the divided signal is impressed on the adder circuit.

3. Simulation Results

In this simulation, we use the four stages M sequence generator, so we have two types of PN sequence pattern, that is, $\{101011001000111\}$ and $\{100010011010111\}$. Table 3 summarizes the simulation conditions of matched filter.

Figure 4 shows the simulation results of the proposed matched filter. From the simulation results, it is found that the proposed matched filter outputs the correctly colleration peak under the given conditions. We found also that the power consumption of the proposed filter is 47.3mW.

4. Experimental Results

The proposed matched filter has been realized in a 1.2 μm CMOS 5 V technology with two metal layers and two polysil-

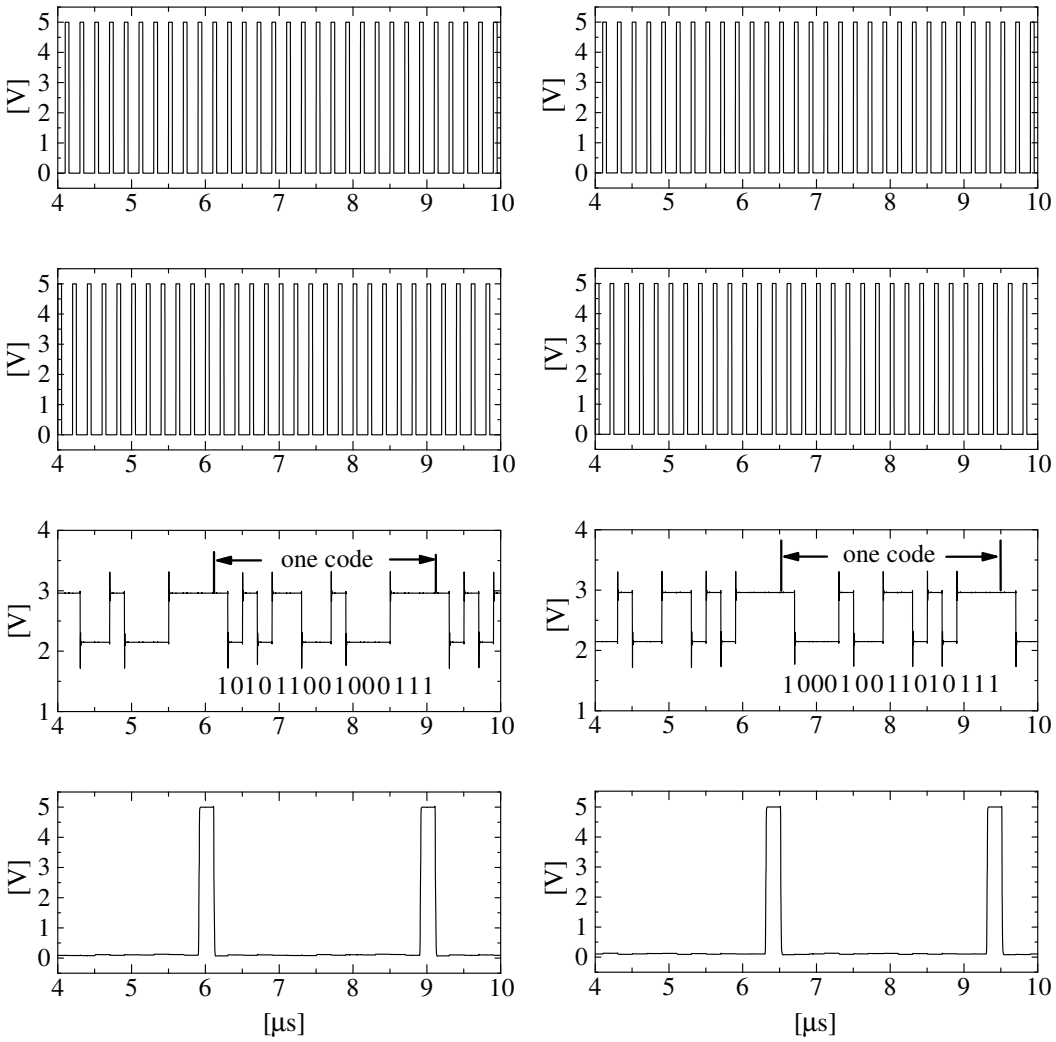

Figure 4. Simulation results.

Table 3. Simulation conditions.

Name		Value	
SH clock		ϕ_1	ϕ_2
	initial value [V]	0	0
	pulse value [V]	5	5
	delay [ns]	100	0
	pulse width [ns]	50	50
	period [ns]	200	200
input signal			
	frequency [MHz]	5.0	
	offset [V]	2.5	
	amplitude [V]	1.0	

icon layers. This chip is 2.3×2.3 mm^2 and is mounted in the 80-pin SQFP. Figure 5 shows the photomicrograph of the matched filter chip. This matched filter area without the test vector part is 861×1120 $\mu\mathrm{m}^2$.

As a result of the evaluation, it is found that the spread signal is exactly shifted to the final stage by the sample hold circuit.

5. Conclusions

In this paper, we have presented a new matched filter using a voltage follower realized by using an OP-amp. From the simulation results, we have found that the matched filter with 47.3 mW of power consumption is realized by using a 1.2 μm standard CMOS process.

Acknowledgment

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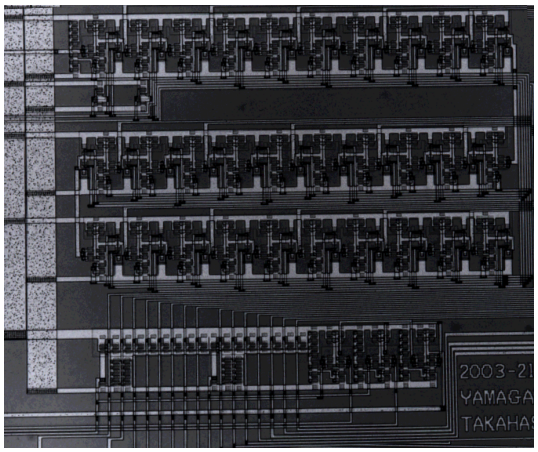

Figure 5. Photomicrograph of matched filter chip.

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