2PADCL: Two Phase drive Adiabatic Dynamic CMOS Logic

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***Abstract*— This paper proposes a novel two-phase drive adiabatic dynamic CMOS logic circuit (2PADCL). The proposed 2PADCL uses two complementary sinusoidal power supply clocks and resembles behavior of static CMOS. As a result, the delay time of the 2PADCL is shorter than that of the conventional ADCL circuit in the second and subsequent stages. The structure of 2PADCL can be also directly derived from static CMOS logic circuits. From the simulation results, we show that the energy consumption of the 2PADCL circuit is lower than those of other diode based adiabatic logic circuits.**

***Keywords*—adiabatic logic, low power, two-phase power supply**

I. Introduction

Adiabatic logic circuit is a new promising approach, which has been originally developed for low power digital circuits [1]–[9]. In many of the earlier papers, the proposed circuits were based on a dynamic operation which calls for four phase power clocking [1], [3], [4]. This type of adiabatic logic suffers from major drawbacks: its clock driver is difficult to design and it cannot provide pipelining. Denker *et al*. [2], Lau *et al*. [5] and Ye *et al.* [6] have presented two-phase drive adiabatic logics, however, these systems require complex circuitry and wire connection for power supply. Adiabatic dynamic CMOS logic (ADCL) is a diode based adiabatic logic which uses one clock supply and is useful for low energy systems [7]–[9]. However, the delay time of each gate is a half period with respect to the periodic power supply voltage in the ADCL circuit. This delay time makes a very clear prediction in regard to the problem difficulty: the larger the number of gate stages becomes, the lower the operating speed of the ADCL [8, Sect. 2]. The ADCL circuit requires also the load capacitor to hold the output voltage [7]. The increase in electric charge/discharge leads to the increase in thermal loss caused by On-state resistance of MOS transistor. Therefore, the design of ADCL logics still requires complex circuits from aspect of hardware implementation.

In this paper, we propose a new topology for the adiabatic dynamic circuit in order to solve the delay problem and the hardware complexity. We also propose a new scheme of generating supply clocks based on the voltage controlled oscillator. The proposed circuit is called two-phase drive adiabatic dynamic CMOS logic (2PADCL). The 2PADCL circuits can be directly converted from static CMOS circuits without drastically increasing the circuit complexity. Through computer simulation, we show that the energy consumption of the 2PADCL circuit is lower than those of other diode based adiabatic logic circuits.

II. Adiabatic Logic

Figures 1(a) and (b) show the conventional ADCL inverter [7] and the modified ADCL [9], respectively. In these circuits, since the output voltage V_{out} of ADCL (or modified ADCL) gate is synchronized with the power supply voltage V_p, the operating speed of the ADCL circuits is determined by the frequency of V_p. This means that the larger the number of gate stages, the lower the operating speed of the ADCL. Figure 1(c) shows a SPICE simulation result for the four ADCL inverter-chains. From this figure, we found that the delay generated from the power supply is increasingly stored in the second and subsequent stages.

The proposed 2PADCL inverter is shown in the top of Fig. 2(a), where the inverter is operated with complementary phases of power supply signals. The supply waveform consists of two modes, "evaluation" and "hold," as shown in the bottom of Fig. 2(a). Let us consider the adiabatic mode. When V_p and $\overline{V_p}$ are in evaluate mode, there is conducting path(s) in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged, which resembles to the CMOS circuit. Thus, there is no need to restore the node voltage to 0 (or V_{DD}) every cycle. When V_p and $\overline{V_p}$ are in hold mode, Output node holds its value in spite of the fact that V_p and $\overline{V_p}$ are changing their values. We can find that such is the case by observing the function of diodes and the fact that the inputs of a gate have a different phase with the output. Circuits node are not necessarily charging and discharging every clock cycle, reducing the node switching activity substantially as shown in Fig. 2(b). Therefore, the speed of 2PADCL circuits is faster than that of ADCL circuits.

The minimum energy consumption in a single inverter is reached when the phase difference between the power supply and the input data is $\pi/2$-rad so that the data is lacking

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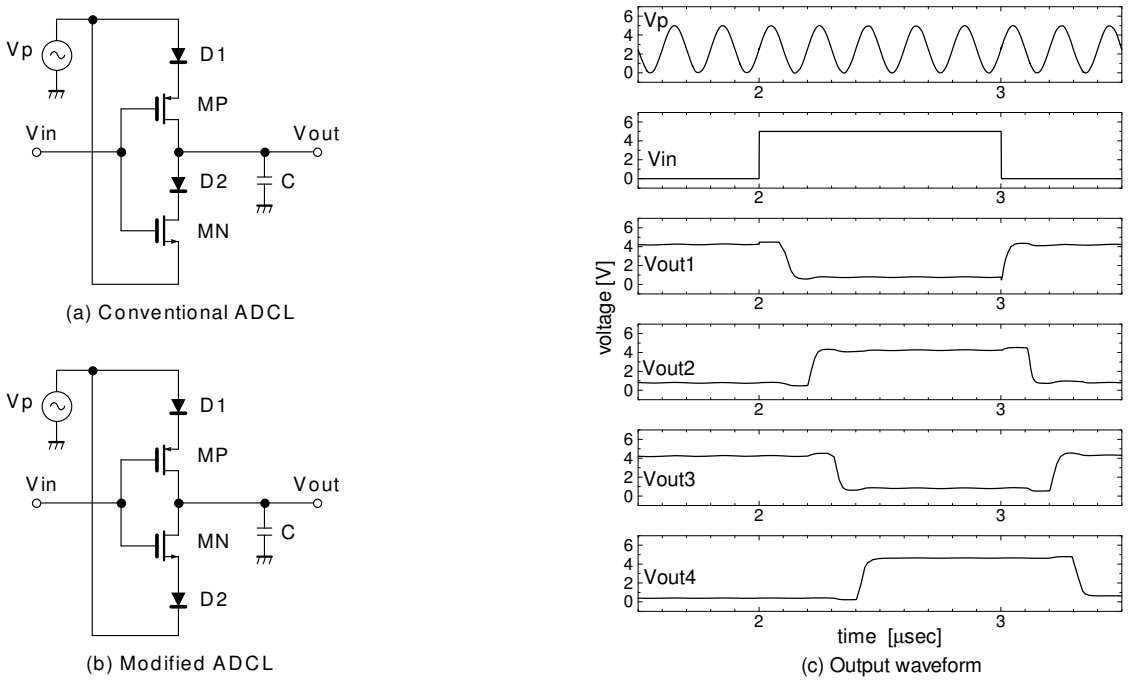


Fig. 1. Adiabatic dynamic CMOS logic (ADCL) and simulated waveform of four ADCL inverter-chains.

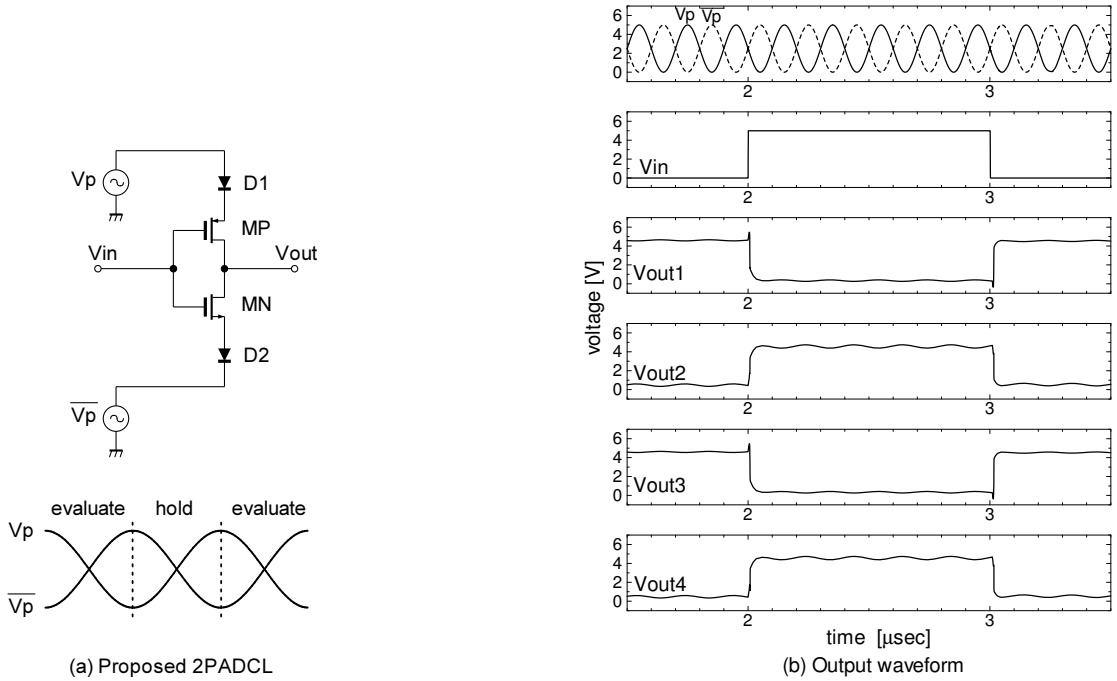


Fig. 2. Two-phase drive ADCL (2PADCL) and simulated waveform of chain of four 2PADCL inverters.

the power supply. When the phase difference is somewhere between 0-rad and $\pi/2$-rad, the slope of the toggling gate's output is partially in CMOS and partially in adiabatic mode. If the phase difference is thought to be determined by a stochastic process, the functionality of the 2PADCL gate is guaranteed only by the following equation: $f_{clk} > f_s$ where f_{clk} and f_s are the frequency of power supply and the frequency of input signal, respectively. In practice the clocking ratios $f_{clk}/f_s \in \{5, 6, 7, 8, 9, 10\}$ can provide about from 80 to 90% adiabatic operation[1]. Therefore, if we select

[1]The 2PADCL inverter having output transition $0 \rightarrow 1$ or $1 \rightarrow 0$ has only shown in the simulation. Just as the inverter is compatible with adiabatic mode under the condition of the phase difference between 0-rad and $\pi/2$-rad, other gates (e.g. 2input-NAND, NOR) and complex gates operate with adiabatic mode under the same condition.

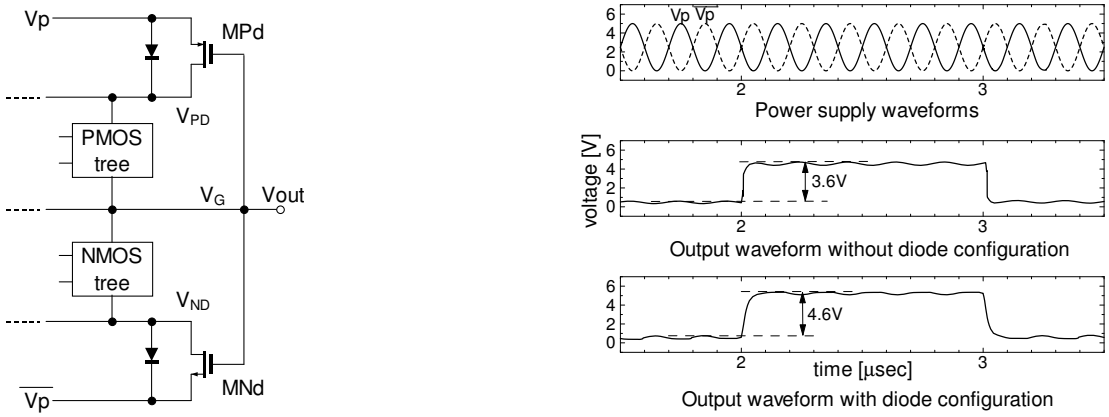


Fig. 3. 2PADCL systems with the diode configuration.

the above ratios (as close to unity as possible), we can reduce the energy consumption of 2PADCL gate. Since 2PADCL gate also is possible to maintain the output voltage without the load capacitor, its energy consumption can be more reduced.

Other feature of the 2PADCL is that the logical "1" state does not reach the peak value of the power supply but is lower by the amount of drain-source voltage V_{DS} of the MOS-switch and the diode voltage V_d, i.e. $V(1) = V_p - V_{DS} - V_d$. In a similar manner, the logical "0" state is not equal to the ground potential but remains above that, i.e. $V(0) = V_{DS} + V_d$. This feature causes that the noise margin is lower than in the CMOS gate, and therefore, the 2PADCL gates are more prone to noise than corresponding CMOS gates. The disadvantage of lower noise margin is avoided by using the effective resistance as shown in Fig. 3(a). In this figure, the voltage drop $V_{PD} - V_G$ across the PMOS tree when charging (and $V_G - V_{ND}$ across the NMOS tree when discharging) results in larger gate-to-source voltage. Hence, with the diode configuration of Fig. 3(a), the voltage drop in the charging/discharging path reduces the effective resistance of P_d and N_d. In the bottom of Fig. 3(b), we show the output of a 2PADCL inverter when the diode configuration is used. As expected, the output signal has a high noise margin. For the same node, it is lower noise margin when the diode configuration is not used, which is shown in the middle of Fig. 3(b).

III. Simulation

The chain of four inverters was tested by SPICE simulation using a standard 1.2 μm CMOS process technology provided by VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by On-Semiconductor Corporation. The transistor size W/L is $5.0/1.2$ for both of the PMOS and NMOS transistors. In the simulation the clocking ratio $f_{clk}/f_s = 5$ was used.

To evaluate the power savings in the circuits, we compute the energy consumption E, which is defined as follows:

$$E = \int_0^{T_s} \left(\sum_{i=1}^{n} (V_{p_i} \times I_{p_i}) \right) dt, \tag{1}$$

where T_s $(=1/f_s)$ is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current, and i is a number of power supply. Therefore, E is equal to the net energy flowing into the circuit from the power supply line.

Figure 4 shows the comparison of energy consumption of different diode based adiabatic logic families; 2N-2N2D [2], ADL [3], APDL [5], QSERL [6], ADCL [7] and proposed 2PADCL. Some points not drawn on the graph represent malfunction due to incomplete adiabatic mode. This result shows that the proposed 2PADCL reduces the energy consumption by about two (or four) times as compared to other adiabatic logics in the 1 MHz to 10 MHz range.

IV. Supply Clock Generation

2PADCL saves the energy by returning delivered energy back to the supply. The AC-power supply is needed to efficiently restore the charge, and so we should design an efficient clock circuit which converts DC power to AC. Figure 5 shows the supply clock generation circuit based on the voltage controlled oscillator (VCO). This supply clock generation circuit comprises of the voltage reference, the current mirror and the LC cross coupled oscillator, and then produces two supply clocks which have 180° phase difference. The free-running frequency f_{clk} is determined according to the following equation:

$$f_{clk} = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}. \tag{2}$$

The complete clock generator circuits are designed with the device parameters shown in Fig. 5, and has a frequency f_{clk} of 10 MHz. From simulations the generator has an energy conversion efficiency of 97%, and then the provided sinusoidal supply voltages are shown in Fig. 6.

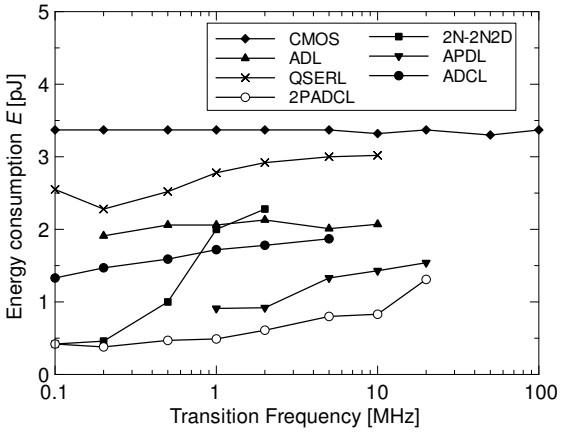
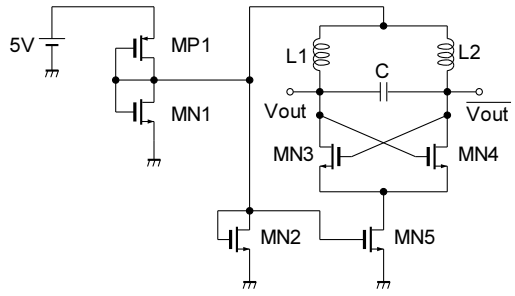


Fig. 4. Energy consumption of different diode based adiabatic logics and CMOS logic.



Device parameter

	W/L [μm]		W/L [μm]
MN1	5/5	MN5	5/15
MN2	5/30	MP1	5/2
MN3, MN4	5/10		
L1, L2	125μH	C	1pF

Fig. 5. Voltage controlled oscillator for generating adiabatic power supply/clocks, achieving an energy conversion efficiency of 97%.

Table I summarizes the power dissipation of each functional block of the 2PADCL 100 inverter-chains. To evaluate power dissipation of adiabatic system, simulations were made the following conditions; the free-running frequency of the VCO shown in Fig. 5 was $f_{clk} = 10$ MHz, input clock frequency was $f_s = 1$ MHz and DC supply voltage was $V_{DD} = 5$ V. From the simulation results, 75.4% power saving is achieved compared to a conventional CMOS.

V. Conclusions

In this paper, we have presented the two-phase drive adiabatic dynamic CMOS logic and a low-energy diode based adiabatic logic family. The performance of 2P-ADCL has short switching delay and relatively high throughput as compared with that of ADCL. Our simulation result with 2PADCL circuits has indicated a factor of from two to four reductions in energy consumption. The power consumption of a complete adiabatic system, including the generation of the clocked supply voltages by means of a two-phase power clock generator with 97% efficiency, has been about 75% lower than the equivalent static CMOS implementation at $f_s = 1$ MHz.

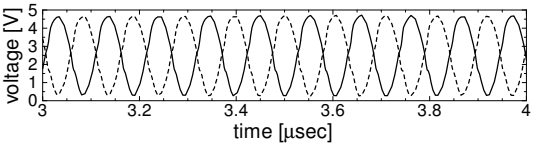


Fig. 6. Output voltages of the adiabatic power supply circuit.

TABLE I
Summary of power dissipation of 100 inverter-chains operating at 1 MHz.

2PADCL 100 inverter-chains core	17.2 μW
Power supply circuit	165 μW
Total Delivered Power	182 μW
Conventional CMOS 100 inverter-chains	742 μW
Power Gain of 2PADCL over CMOS	75.4%

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