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Carry Propagation Free Adder/Subtracter Using Adiabatic Dynamic CMOS Logic Circuit Technology

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SUMMARY This paper describes a design of a Carry Propagation Free Adder/Subtracter (CPFA/S) VLSI using the Adiabatic Dynamic CMOS Logic (ADCL) circuit technology. Using a PSPICE simulator, energy dissipation of the ADCL 1 bit CPFA/S is compared with that of the CMOS 1 bit CPFA/S. As a result, energy dissipation of the proposed ADCL circuits is about 1/3 as high as that of the CMOS circuits. The transistors count, propagation-delay time and energy dissipation of the ADCL 4 bit CPFA/S are compared with those of the ADCL 4 bit Ripple Carry Adder/Subtracter (RCA/S). The transistors count and propagation-delay time are found to be reduced by 7.02% and 57.1%, respectively. Also, energy dissipation is found to be reduced by 78.4%. Circuit operation and performance are evaluated using a chain of the ADCL 1 bit CPFA/S fabricated in a 1.2 μm CMOS process. The experimental results show that addition and subtraction are operated with clock frequencies up to about 1 MHz. In addition, the total power dissipation of the ADCL 1 bit CPFA/S is 28.7 μW including the power supply.

key words: *adiabatic dynamic CMOS logic (ADCL), carry propagation free, adder/subtracter, VLSI, redundant binary*

1. Introduction

Demands for low power and low noise digital circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. The Adiabatic (Energy-recovering) logic is a new promising approach, which has been originally developed for low power digital circuits [1]–[6]. In particular, the Adiabatic Dynamic CMOS Logic circuit (ADCL) [5] achieves ultra low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors. It is known that output voltage of the ADCL gates is synchronized with the power supply voltage. For the reason, the larger the number of gate stages increases, the lower the operating speed of the ADCL becomes. Especially, the ADCL circuit using the Carry propagation Adder/Subtracter (CPA/S) causes a serious problem.

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On the other hand, the Redundant Binary (RB) number system has the trait of the Carry propagation Free Adder/Subtracter (CPFA/S) [7]–[11]. Because the operations of the RB system consist of the iterative and successive additions/subtractions, they are applied to the complicated arithmetic multiplier units included in the FIR Hilbert Transformer [12].

In this paper, first, we propose a new adder/subtracter with shorter propagation-delay time. This adder/subtracter consists of modified CPFA/S suitable for ADCL circuit technology. Secondly, we show the simulation results concerned with the 1 bit CPFA/S and 4 bit CPFA/S realized by using the ADCL and the CMOS logic. Finally, we verify that carrying out design, trial manufacture and evaluation using the ADCL circuit actually, in respect of the CPFA/S integrated circuit, ensure the effectiveness of ADCL circuit technique.

2. Basic Logic Using ADCL Circuit

An ADCL inverter gate (ADCL–NOT) is shown in Fig. 1. In this circuit, since the output voltage V_{OUT} of the ADCL gate is synchronized with the power supply voltage V_ϕ, the operating speed of the ADCL circuits is determined by the frequency of V_ϕ. The principle of ADCL–NOT is shown in Fig. 2.

Principle (a) V_{IN} : H→L
In Fig. 2(a), the pMOS (MP_1) and the nMOS (MN_1) are ON and OFF, respectively. In this case, the supply

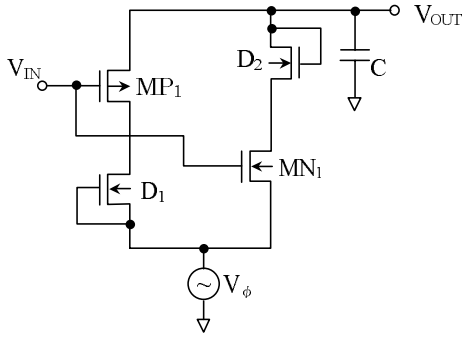
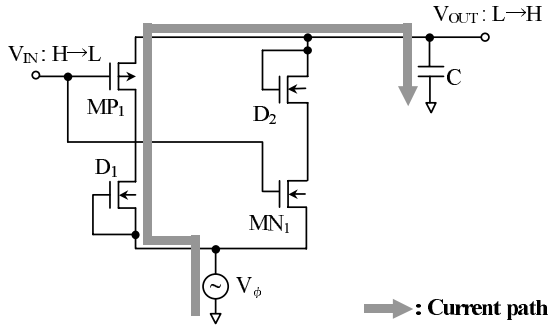
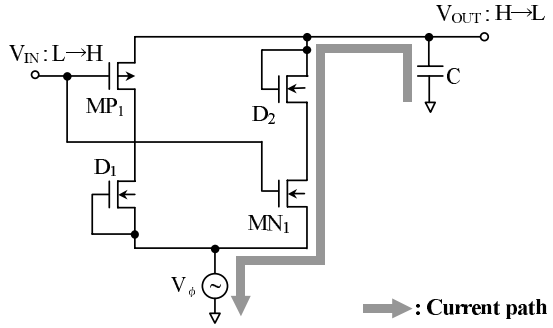


Fig. 1 ADCL inverter gate (ADCL–NOT).



(a) H output.



(b) L output.

Fig. 2 Supply current paths in ADCL–NOT.

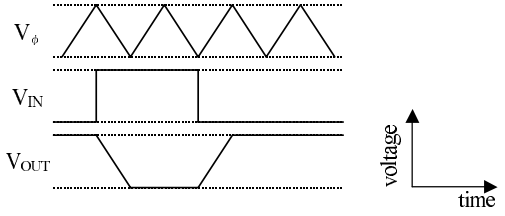


Fig. 3 Output waveform of ADCL–NOT in adiabatic mode.

current path is generated and the load capacitor C is charged by V_ϕ.

Principle (b) V_{IN} : L→H
In this condition, conversely, MP_1 and MN_1 are OFF and in the ON, respectively. It leads that the current path as shown in Fig. 2(b) is generated and the charge in C is redrawn into V_ϕ.

When the operation of a circuit is based on Principles (a) and (b), this circuit functions as ADCL–NOT. However, if the difference between V_ϕ and the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated. Consequently, ADCL–NOT works in the *adiabatic mode* as delineated in Fig. 3. The output voltage V_{OUT} is delayed by 0.5 period per gate of the power supply voltage V_ϕ in the ADCL circuit. Therefore, the propagation-delay time unit (i.e. critical pass length) Δ_ϕ for the ADCL circuit is defined as:

Table 1 Propagation-delay time of ADCL circiut.

Logic name	Propagation-delay time
ADCL–NOT	$1\Delta_\phi$
2input ADCL–NAND	$1\Delta_\phi$
2input ADCL–NOR	$1\Delta_\phi$
2input ADCL–ExOR	$2\Delta_\phi$
2input ADCL–ExNOR	$2\Delta_\phi$

$$\Delta_\phi = \frac{1}{2}\mathrm{T}_\phi \tag{1}$$

where T_ϕ is the period of the power supply voltage. As a result, an ADCL–NOT has propagation-delay time of $1\Delta_\phi$. The other propagation-delay time of the ADCL circuits are summarized in Table 1.

3. Carry Propagation Free Adder/Subtracter

3.1 Redundant Binary Representation

The RB representation used in this paper is one of the Signed-Digit (SD) representation proposed by Avizienis [7]. It has a fixed radix-2 and a digit set $\{\overline{1},0,1\}$ where $\overline{1}$ denotes -1. The radix-2 SD code representation of a fractional number X has the general form:

$$X = \sum_{k=0}^{N-1} x_k 2^k \tag{2}$$

where $x_k \in \{\overline{1}, 0, 1\}$. N is the number of ternary digits. The RB representation allows the existence of redundancy. For example, integer "−3" is expressed as:

$$\begin{aligned}[-3]_{10} &= [\,0\,0\,\overline{1}\,\overline{1}\,]_{\mathrm{SD}} \\ &= [\,0\,\overline{1}\,0\,1\,]_{\mathrm{SD}} \\ &= [\,0\,\overline{1}\,1\,\overline{1}\,]_{\mathrm{SD}} \\ &= [\,\overline{1}\,1\,0\,1\,]_{\mathrm{SD}} \\ &= [\,\overline{1}\,1\,1\,\overline{1}\,]_{\mathrm{SD}}\end{aligned} \tag{3}$$

We can compose the CPFA/S using the above redundancy.

3.2 Structure of CPFA/S

The CPFA/S between two SD number, that is to say augend X and addend Y, is performed in i-th place by the following steps:

$$\textbf{step1}: \quad x_i + y_i = 2c_i + s_i \tag{4a}$$

$$\textbf{step2}: \quad z_i = s_i + c_{i-1} \tag{4b}$$

where c_i is intermediate carry, s_i is intermediate sum, z_i is final sum and c_i, s_i, $z_i \in \{\overline{1}, 0, 1\}$. Any arithmetic operation can be defined by a table which contains all possible pairs of digits and by a corresponding table entry which defines the outcome of the operation. In terms of addition, such tables are referred to as *addition tables* and contain all possible combinations of the addend and augend with a corresponding sum digit.

Table 2 Computation addition table.

Type	x_i	y_i	x_{i-1}, y_{i-1}	c_i	s_i
(a)	$\overline{1}$	$\overline{1}$	———	$\overline{1}$	0
(b)	0	$\overline{1}$	Both are non-negative.	0	$\overline{1}$
	$\overline{1}$	0	Otherwise	$\overline{1}$	1
(c)	1	$\overline{1}$	———	0	0
(d)	$\overline{1}$	1	———	0	0
(e)	0	0	———	0	0
(f)	0	1	Otherwise	0	1
	1	0	Both are non-negative.	1	$\overline{1}$
(g)	1	1	———	1	0

Therefore, Eq. (4) can be given as *addition tables*. One of the first binary addition tables is given in [9]. Table 2 is a reproduction of the addition table summarized in [9]. In this table, each sum is represented as s_i and c_i. In the rows (b) and (f), s_i and c_i are determined by the arithmetic signs of x_{i-1} and y_{i-1}. These two digits are part of the intermediate values combined with a guarantee of no ripple in the final stage. In this way, the final step which combines the intermediate carry with sum digits to form a final sum can be accomplished with a guarantee that no carry ripples will occur.

Figure 4 depicts the CPFA/S building block. This building block consists of standard Boolean logic. In Fig. 4(a), Cell1 uses two ExNOR gates. The conventional ADCL–ExNOR shown in Fig. 5(a) have been consisted of NAND gate and NOR-NOT-NAND gate, which means that its propagation-delay time is $3\Delta_\phi$. On the other hand, the proposed ADCL–ExNOR shown in Fig. 5(b) is consisting of product of sums (POS) circuits, and this proposed circuit becomes propagation-delay time of $2\Delta_\phi$. Therefore, its propagation-delay time is shorter than that of the conventional one, which means that the proposed circuit is suitable for ADCL circuit technology.

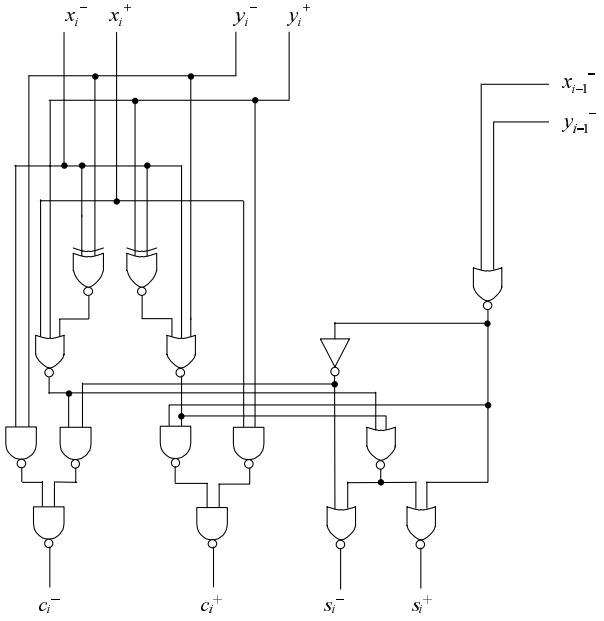
In Fig. 4, digit set $\{\overline{1}, 0, 1\}$ are expressed as:

$$[\,\overline{1}\,] = [\,x_i^-, x_i^+] = [\,1\,,\,0\,] \tag{5a}$$

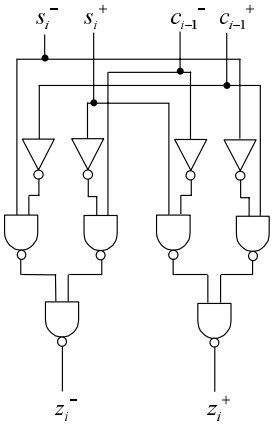
$$[\,0\,] = [\,x_i^-, x_i^+] = [\,0\,,\,0\,] \tag{5b}$$

$$[\,1\,] = [\,x_i^-, x_i^+] = [\,0\,,\,1\,] \tag{5c}$$

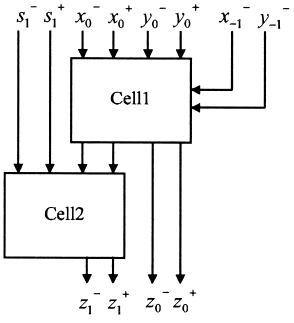
The Cell1 and Cell2 generate intermediate carry and intermediate sum, respectively. The adder/subtracter of arbitrary length can be realized by using parallel connection of the block diagram shown in Fig. 4(c). The CPFA/S always ensures constant propagation-delay time. In this case, maximum propagation-delay time of the CPFA/S using the ADCL circuits is less than $8\Delta_\phi$.



(a) Intermediate carry logic (Cell1).



(b) Intermediate sum logic (Cell2).



(c) 1 bit CPFA/S.

Fig. 4 CPFA/S building block.

4. PSPICE Simulation Results

4.1 Energy Dissipation of 1 bit CPFA/S

Figure 6 shows the comparison of energy dissipation of the CMOS 1 bit CPFA/S and the ADCL 1 bit CPFA/S. The conditions of PSPICE simulator are following:

CMOS 1 bit CPFA/S:
supply voltage V_{dd} : 2 V †, DC

clock frequency f : 5 V, 1 MHz, square wave

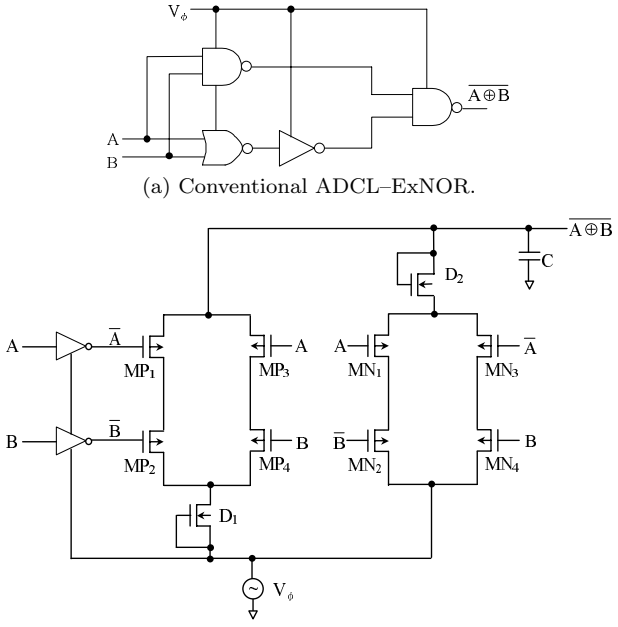
ADCL 1 bit CPFA/S:

supply voltage V_{dd} : 5 V, DC
supply voltage V_ϕ : 5 V, 10 MHz, sine wave
clock frequency f : 5 V, 1 MHz, square wave

From this result, we find that the energy dissipation of the ADCL 1 bit CPFA/S is about 1/3 as high as that of the CMOS 1bit CPFA/S.

4.2 Comparison for 4 Bit Adder/Subtracter

In [13], the ADCL 4 bit CPA/S is designed to implement a 2's complement Ripple Carry Adder/Subtracter (RCA/S). Since the ADCL 4 bit RCA/S has long propagation-delay time, the clock speed is the main problem. On the other hand, the CPFA/S has a certain propagation-delay time. Table 3 summarizes transistors count, maximum propagation-delay time and energy dissipation of the 4 bit adder/subtracters. In this table, CLA/S and CSA/S stand for Carry Look-ahead Adder/Subtracter and Carry Select Adder/Subtracter, respectively. It is clear that CPFA/S is superior to RCA/S in all parameters in Table 3. In addition, CPFA/S is superior to another adder/subtracter in maximum propagation-delay time and energy dissipation. For a standpoint of propagation-delay time and energy dissipation, it can be concluded that the "ADCL Adder/Subtracter" is suitable for realizing the "CPFA/S."



(a) Conventional ADCL–ExNOR.

(b) Proposed ADCL–ExNOR of POS circuits.

Fig. 5 ExNOR gates for ADCL circuit technology.

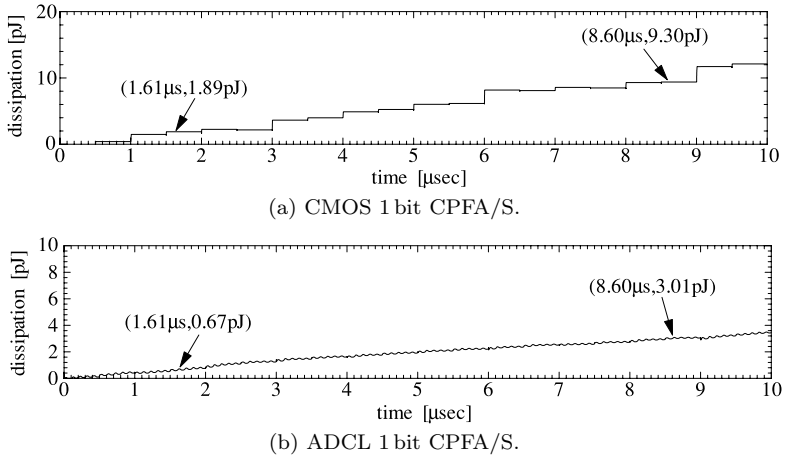
5. 1 Bit CPFA/S VLSI Fabrication of ADCL Technology

The 1 bit CPFA/S VLSI using the ADCL circuit was fabricated by using a 1.2 μm CMOS process. This chip size is $2.3 \times 2.3\,\text{mm}^2$ and is mounted in 52-pin SQFP. The transistor size W/L is 5.0 μm/1.2 μm for both of the pMOS and the nMOS transistors. The element value of the ADCL load capacitor to hold the output voltage is 0.05pF. In the input and the output interfaces, the conventional CMOS circuits are used in order to realize the CMOS interface compatibility. Therefore, these interface circuits are non-adiabatic. Figure 7 shows the photomicrograph of the ADCL 1 bit CPFA/S chip. This ADCL 1 bit CPFA/S area without the test vector part is $370 \times 740\,\mu\text{m}^2$.

5.1 Operational Speed

Figures 8 and 9 display the results of PSPICE simulation and the results of measurement, respectively. In

†In this paper, the threshold voltage of pMOS (V_{Tp}) and NMOS (V_{Tn}) are −0.9 V and 0.82 V, respectively. Therefore, under this condition, the minimum operating supply voltage of CMOS circuit is about 2 V.



(a) CMOS 1 bit CPFA/S.

(b) ADCL 1 bit CPFA/S.

Fig. 6 Energy dissipation for PSPICE simulation.

Table 3 Comparision for 4 bit CPA/Ss and 4 bit CPFA/S.

	Transistors count	Maximum propagation -delay time	Energy dissipation per one operation
(a) RCA/S	684	$21\Delta_\phi$	119 pJ
(b) CLA/S	448	$11\Delta_\phi$	32.5 pJ
(c) CSA/S	716	$15\Delta_\phi$	51.5 pJ
(d) CPFA/S (+ RB to binary converter)	636 (+64)	$8\Delta_\phi$ ($+2\Delta_\phi$)	25.7 pJ (+1.2pJ)
Reduction ratio : $\left(1-\frac{(d)}{(a)}\right)\times 100$ [%] (not include RB to binary converter)	**7.02**	**57.1**	**78.4**

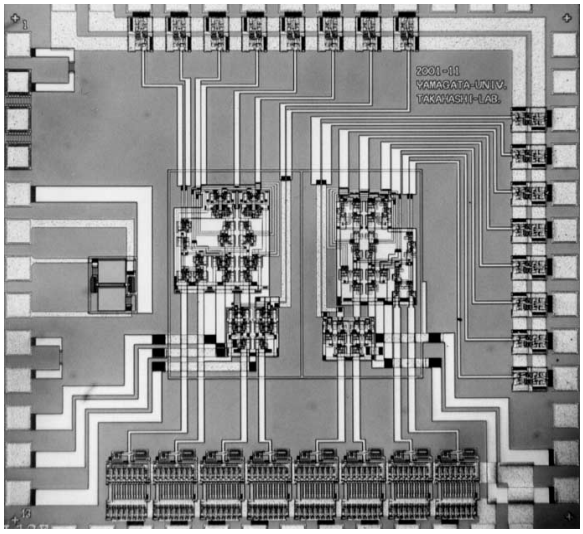


Fig. 7 Photomicrograph of 1 bit adder/subtracter chip.

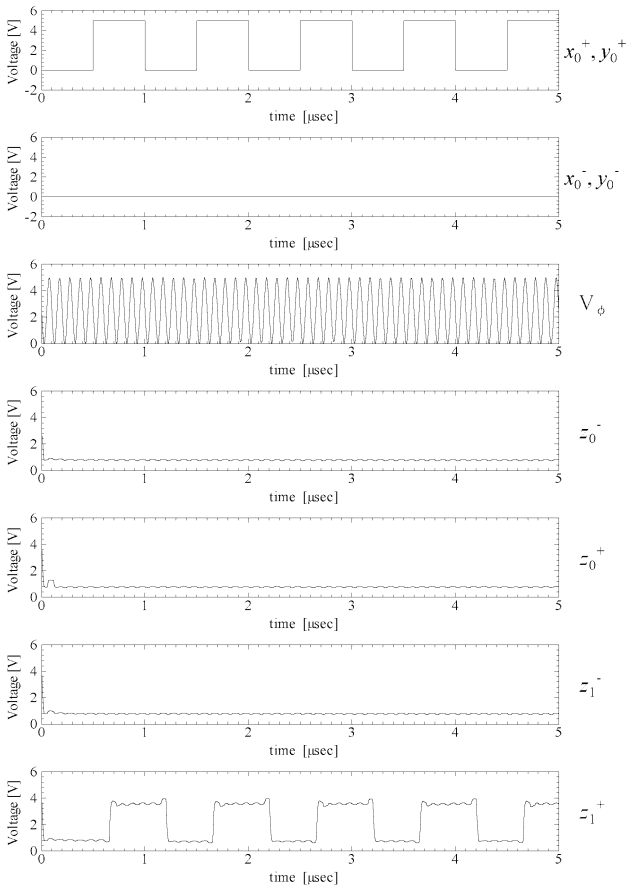


Fig. 8 Results of PSPICE simulation (1 + 1 operation).

both of computer simulation and experiment, the supply voltage and clock frequency are as follows.

supply voltage V_{dd} : 5 V, DC
supply voltage V_ϕ : 5 V, 10 MHz, sine wave
clock frequency f : 5 V, 1 MHz, square wave

Comparing Fig. 8 with Fig. 9 shows that the observed values agree well with the simulated ones. Moreover, it is found that the ADCL 1 bit CPFA/S is operating correctly with clock frequencies up to about 1 MHz.

5.2 Power Dissipation

In order to verify the power dissipation of the proposed ADCL 1 bit CPFA/S, we used the power supply circuit illustrated in Fig. 10 [14]. This circuit is based on the Clapp oscillator that generates the sinusoidal voltage. This circuit is realized by using discrete components. In Fig. 10, the MOS transistor 2SK241 is normally-on type, thereby reducing the DC power supply voltage. The current flows out from the circuit shown in Fig. 10 is set by adjusting the source resistance 330 Ω in order to generate the sinusoidal power supply whose voltage is $5V_{pp}$ at the output terminal V_ϕ. The frequency of V_ϕ is controlled to be near 10 MHz by adjusting the element values of L or C.

The oscillator circuit shown in Fig. 10 is connected to the ADCL 1 bit CPFA/S for supplying the power and thus, the ADCL system is constructed. The ADCL system is experimentally confirmed to operate perfectly. Dependency of the ADCL system power dissipation on the DC power supply voltage is shown in Fig. 11. From the figure, it is found that the ADCL system can op-

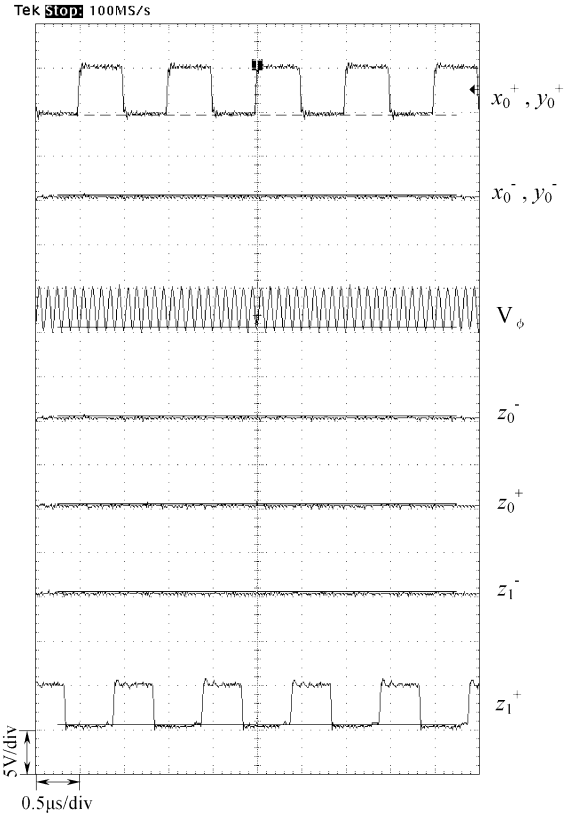


Fig. 9 Results of measurement (1 + 1 operation).

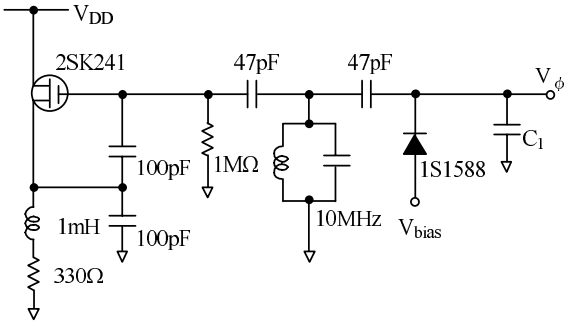


Fig. 10 Clapp oscillator circuit for supplying the power to ADCL 1 bit CPFA/S.

erate with sub-one volt DC power supply and that the minimum power dissipation is 28.7 μW at the 1.3 V DC power supply voltage.

The power dissipation described in this paper is of the ADCL 1 bit CPFA/S. Therefore, the power dissipation of the ADCL n-bit CPFA/S would be n times as high as that of the ADCL 1 bit CPFA/S.

6. Conclusion

In this paper, the Carry propagation Free Adder/Subtracter (CPFA/S) scheme using ADCL technology is presented. It is shown that energy dissipation of the ADCL 1 bit CPFA/S is about 1/3 as high as that

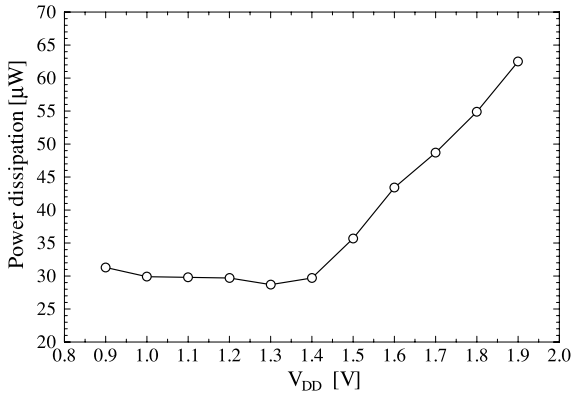


Fig. 11 Dependency of the ADCL system power dissipation on the DC supply voltage.

Table 4 ADCL 1 bit CPFA/S Chip feature summary.

Feature	Value
Maximum Clock Frequency	1 MHz
Technology	1.2 μm N-well CMOS, 2metal, 2poly
Transistors	174
Transistor size W/L	5.0 μm/1.2 μm
Test vector Area	370 × 740 μm^2
Die area	2.3 × 2.3 mm^2
Total power dissipation including power supply	28.7 μW@1 MHz, 1.3 VDC

of the CMOS 1 bit CPFA/S through PSPICE simulation. And, maximum propagation-delay time for the CPFA/S is found to be $8\Delta_\phi$. The ADCL 1 bit CPFA/S is implemented by using a 1.2 μm CMOS process technology with the area of 370 × 740 μm^2. The experimental results show that addition and subtraction are operated with clock frequencies up to about 1 MHz. Additionally, the total power dissipation of the ADCL 1 bit CPFA/S is 28.7 μW including the power supply.

Acknowledgement

The ADCL 1 bit CPFA/S chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by On- Semiconductor, Nippon Motorola LTD., HOYA Corporation, and KYOCERA Corporation.

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